CMS TBM05 Wafer Test Description and Results

Cristian Gingu
Fermi National Accelerator Laboratory, Batavia, IL 60510
- October 2005 -

Introduction

This document is a technical report of the TBM05 chip wafer test results. Five wafers were tested, which are identified below as: wafer #1 (ID=MIFR49T), wafer #2 (ID=XG4INAT), wafer #3 (ID=MDFR4ET), wafer#4 (ID=MEFR4DT) and wafer#5 (ID=MBFR4GT).

An overview of TBM testing program is presented in Section 1. Details about each test procedure are given in Section 2. Section 3 describes how the test report files are organized. Test results for the 5 mentioned wafers are presented briefly in Section 4 and the attached Excel file provides convenient data analysis and some graphics and histograms.

1. Test program overview

The TBM testing program is based on the test procedure suggested by chip designer. Most of the tests were slightly modified from the original ones to accommodate hardware particularities. Some tests were not implemented because of hardware limitations. Some other tests are new. The overall testing program flow is presented below. The new tests are in italics.

GROUP 1. Hub and Ports
T11PowerSupply
T12Registers
T13ROCPorts
T14HubAddress

GROUP 2. TBM Triggers
T20CalibModeCSRTrig
T21SyncModeNormTrigg
T22SyncModeCSRTrigg
T23ClearEventCounterModeNormTrigg
T24ClearEventCounterModeCSRNormTrigg
T25ClearEventCounterModeROCResetTrigg
T26ClearEventCounterModeNormTrigg

T27ClearEventCounterModeTBMResetTrigg
T28ClearEventCounterModeNormTrigg
T29ReadoutMode20MHz

GROUP 3. Stack
T31TBMStack32NormTrigg
T32TBMStack32StackCount
T33TBMStack32StackEvent
T34TBMStack32ReadVerify
T35TBMStack24NormTrigg
T36TBMStack24ReadVerify

GROUP 4. Analog Output
T41ScanRegAnaInpBias
T42ScanRegAnaOutBias
T43ScanRegAnaOutGain
T44RiseFallTimesP0
T45RiseFallTimesP1
T46RiseFallTimesP2
T47RiseFallTimesP3
T48PulseLinP0
T49PulseLinP2

GROUP 5. Single TBM
T51SingleTBMA
T51SingleTBMAOnly
T52SingleTBMB
T52SingleTBMBOnly

GROUP 6. Miscellaneous
T61IgnoreIncommTrigg
T62DisableTrigg
T67InjectROCResetTriggTBMA
T68InjectROCResetTriggTBMB
T69InjectCalibTriggTBMA
T70InjectCalibTriggTBMB
T71InjectTBMResetTriggTBMA
T72InjectTBMResetTriggTBMB
T73ClearStackCounter

All tests are executed in this order, regardless of the results of previous tests, with the following exception of T11 which, if failed, testing program is aborted.

The test results are reported using Failure Codes associated with each test, or miscellaneous calculated values as rise time and fall time or simply raw measurement values

for later analysis. There are three text files that contain this information, structured as follows:

1. There is one file associated with each TBM chip. This is the basic report file and it can be configured to report the information at different detail levels. It is very helpful in code development and also for in depth analysis of measured data, when needed. For example the file named MBFR4GT_10_1.txt reports test data for TBM chip#1 on reticule#10 on wafer ID=MBFR4GT. All the report examples in the following section belong to this type of file.
2. Another file, named for example MBFR4GT_WaferData.txt contains brief test results for all chips on wafer ID=MBFR4GT. This is very handy in giving a pass / fail overview of all chips on the specified wafer. It can also be easily imported in Excel where the data analysis tool can be used for further investigations.
3. Another file, introduced later, named for example MBFR4GT_WaferDataAna.txt contains miscellaneous analog tests results for all chips on wafer ID=MBFR4GT.

We will come back to the last two files with more details in Section 3. Note also that *.xml files were later defined for CMS data base purpose.

2. Test program description

T11PowerSupply test description

The following currents and voltages are measured. The acceptance values are also listed below. This test is performed at the very beginning, after powering on the chip and issuing a TBM hardware reset.

Idig = 5 to 15 mA
Iana = 10 to 25 mA for TBM05, 5 to 15 mA for TBM04
Vcapva = 1.8 to 2.4 V
Vcapvd = 1.8 to 2.4 V
Vcaplvdslow = 0.7 to 1.3 V
Vcaplvdshigh = 0.9 to 1.5 V

The test report looks like the following:

```
************************************************************
9/19/2005    8:14:43 PM    Wafer#MBFR4GT    Chip#4_1
************************************************************
PowerSupplyTest Report
Vdid      =2.487V
Vana      =2.478V
Vcapvd    =2.095V
Vcapva    =2.041V
Vcaplvdslow  =1.021V
```

```
Vcaplvdshigh =1.212V
Idig         =8.72mA
Iana         =17.33mA
PowerSupplyFailCode=0       0  0  0  0  0  0  0  0  0  0  0  0  0
**************************************************************
```

The following is the encoding of the 13 bit long integer PowerSupplyFailCode:
Bit0= software type error
Bit1= Idig too low
Bit2= Idig too high
Bit3= Iana too low
Bit4= Iana too high
Bit5= Vcapva too low
Bit6= Vcapva too high
Bit7= Vcapvd too low
Bit8= Vcapvd too high
Bit9= Vcaplvdslow too low
Bit10= Vcaplvdslow too high
Bit11= Vcaplvdshigh too low
Bit12= Vcaplvdshigh too high

T12Registers test description

This test exercise TBM registers as follows:
1. Read default value, then reset
2. Write 0x55 and read back, then reset
3. Write 0xAA and read back, then reset

This algorithm is applied to all 16 pairs of registers (8 pairs on TBMA, 8 pairs on TBMB). But since not all registers can be tested this way, the decision of PASS/FAIL after this test in implemented only for selected registers (for example in the current implementation the analog bias/gain registers are not included).

The test report looks like the following:

```
**************************************************************
TBMPortRegistersTest Report
E0-E1       00        55        AA
E2-E3       00        40        80
E4-E5       00        00        00
E6-E7       B9        B9        B9
E8-E9       B8        D5        AA
EA-EB       80        80        80
EC-ED       80        80        80
EE-EF       80        80        80
```

```
F0-F1       00        55        AA
F2-F3       00        40        80
F4-F5       00        00        00
F6-F7       B8        B8        B8
F8-F9       B8        FD        BA
FA-FB       BA        FD        BA
FC-FD       B8        FD        BA
FE-FF       B8        FD        BA
TBMPortRegisters_FailCode(E0,E1) = 0      0 0 0 0 0 0 0 0 0
TBMPortRegisters_FailCode(E2,E3) = 0      0 0 0 0 0 0 0 0 0
TBMPortRegisters_FailCode(E4,E5) = 0      0 0 0 0 0 0 0 0 0
TBMPortRegisters_FailCode(E6,E7) = 0      0 0 0 0 0 0 0 0 0
TBMPortRegisters_FailCode(E8,E9) = 0      0 0 0 0 0 0 0 0 0
TBMPortRegisters_FailCode(EA,EB) = 0      0 0 0 0 0 0 0 0 0
TBMPortRegisters_FailCode(EC,ED) = 0      0 0 0 0 0 0 0 0 0
TBMPortRegisters_FailCode(EE,EF) = 0      0 0 0 0 0 0 0 0 0
TBMPortRegisters_FailCode(F0,F1) = 0      0 0 0 0 0 0 0 0 0
TBMPortRegisters_FailCode(F2,F3) = 0      0 0 0 0 0 0 0 0 0
TBMPortRegisters_FailCode(F4,F5) = 0      0 0 0 0 0 0 0 0 0
TBMPortRegisters_FailCode(F6,F7) = 0      0 0 0 0 0 0 0 0 0
TBMPortRegisters_FailCode(F8,F9) = 0      0 0 0 0 0 0 0 0 0
TBMPortRegisters_FailCode(FA,FB) = 0      0 0 0 0 0 0 0 0 0
TBMPortRegisters_FailCode(FC,FD) = 0      0 0 0 0 0 0 0 0 0
TBMPortRegisters_FailCode(FE,FF) = 0      0 0 0 0 0 0 0 0 0
************************************************************
```

The following is the encoding of the 9 bit long integer TBMPortRegisters_FailCode:
Bit0= error of return fifo full bit
Bit1= error of return fifo empty bit
Bit2= error of returned register address
Bit3= error of returned hub and port address
Bit4= error of returned register data when reading default
Bit5= error of returned register data when writing 0x55
Bit6= error of returned register data when reading 0x55
Bit7= error of returned register data when writing 0xAA
Bit8= error of returned register data when reading 0xAA

Only few registers are checked for these errors, and sometimes only some bits of the register are checked for errors, as follows:

E0,E1,F0,F1 reading back values: 0x00,0x55,0xAA
E2,E3,F2,F3 reading back values: 0x00,0x40,0x80 (instead of 0x00,0x55,0xAA)
E8,E9,F8,F9 reading back values: 0x00,0x05,0x02 (instead of 0x00,0x55,0xAA)

All the other registers are not checked for write/read errors and their FailCode will always be 0. If at least one of the above fail code numbers is not zero, the test is considered failed.

T13ROCPorts test description

This test exercises each TBM port address 0,1,2,3 as follows:
1. Set hub address 01 for this test, 40MHz readout mode
2. Send a command with byte2=0x55, byte3=0xAA
3. Check return fifo data
4. Check interface board status register SR1
5. Send one Normal (L1A) trigger
6. Check interface board status register SR1

The interface board status register SR1 contains the following bits assignment:
Bit0= Token Out A signal latched
Bit1= Token Out B signal latched
Bit2= NA
Bit3= NA
Bit4= Return Clock signal present at TBM output
Bit5= Trigger signal latched at the selected TBM port
Bit6= SDA signal latched at the selected TBM port
Bit7= CLK signal latched at the selected TBM port

The test report looks like the following:

```
*************************************************************
ROCPortsTest Report
ROCPortsTest_FailCode(0,X)=0 0  0       000     00000000    00000000
ROCPortsTest_FailCode(1,X)=0 0  0       000     00000000    00000000
ROCPortsTest_FailCode(2,X)=0 0  0       000     00000000    00000000
ROCPortsTest_FailCode(3,X)=0 0  0       000     00000000    00000000
*************************************************************
```

There are three fail code numbers associated with each port number (0, 1, 2, 3) tested.
The first fail code number (see step 3. Check return fifo data) is a 3 bit long integer:
Bit0= error of return fifo full bit
Bit1= error of return fifo empty bit
Bit2= error of returned register address (byte2=0x55) or
error of returned register data (byte3=0xAA) or
error of returned hub and port address (should be 0x0C)

The second fail code number (see step 4. Check interface board status register SR1) is an 8 bit long integer equal with SR1 byte value after sending the I2C command, if the SR1 value is different from the correct value (which is 0xD0 for this case, that means CLK, SDA and Return Clock present). If the value is the correct one, this fail code is zero.

The third fail code number (see step 6. Check interface board status register SR1) is an 8 bit long integer equal with SR1 byte value after sending the trigger, if the SR1 value is different from the correct value (which is 0xA3 for this case)

If at least one of the fail code numbers is not zero, the test is considered failed.

T14HubAddress test description

This test exercises each Hub address as follows:

1. Set the hub address to one of the following values 0x00, 01, 02, 04, 08, 10, 1F.
2. For each of the above 7 hub addresses, send an I2C command ONLY to port 0 with byte2=55, byte3=AA and trying all 32 hub addresses from 0x00 to 0x1F.
3. Check the SR1 register after each I2C command.

The test report looks like the following:

```
**************************************************************
HubAddressTest Test Report
HubAddressTest_FailCode(00,X)=0 0  0    0  0000000000000000  0000000000000000
HubAddressTest_FailCode(01,X)=0 0  0    0  0000000000000000  0000000000000000
HubAddressTest_FailCode(02,X)=0 0  0    0  0000000000000000  0000000000000000
HubAddressTest_FailCode(04,X)=0 0  0    0  0000000000000000  0000000000000000
HubAddressTest_FailCode(08,X)=0 0  0    0  0000000000000000  0000000000000000
HubAddressTest_FailCode(10,X)=0 0  0    0  0000000000000000  0000000000000000
HubAddressTest_FailCode(1F,X)=0 0  0    0  0000000000000000  0000000000000000
**************************************************************
```

There are three fail code numbers associated with this test, for each of the seven hub addresses applied on TBM pads.

The first fail code number is a 1 bit long integer: Bit0= software type error The second fail code number is a 16 bit long integer associated with I2C addresses 0 to 15. The third fail code number is a 16 bit long integer associated with I2C addresses 16 to 31. An error will flag in one of these 16+16=32 positions if:

a) The SR1 value is different from 0xD0 when the I2C address matches the hub port address set on TBM pads.

b) The SR1 value is different from 0x80 when the I2C address is different from the hub port address set on TBM pads.

If at least one of the fail code numbers is not zero, the test is considered failed.

T20CalibModeCSRTrig test description

Before this test T20 the TBM chip is programmed to 40MHz readout speed (write 0x01 in registers E0, F0) and the Clear Event Counter bit is set (write 0x80 in registers E4, F4).

The T20 test consists in following steps:

1. Set Calibrate mode (write 0xC0 in registers E2, F2). Set the CSR trigger type to be sent by the sequencer.
2. For each TBM port address 0,1,2,3 send one trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.

The test report looks like the following:

```
************************************************************
TBMTriggers - CSRTriggers Test Report
ReadoutASICFIFO_FailCode=0   0  0  0
TBMA BaseLine (min,max,avg,range)= 1919    1953        1935        34
TBMB BaseLine (min,max,avg,range)= 2082    2098        2090        16
TBMA UltraBlk (min,max,avg,range)= 1918    1951        1934        33
TBMB UltraBlk (min,max,avg,range)= 2081    2095        2088        14
TBMA AnaLev_0 (min,max,avg,range)= 1920    1953        1935        33
TBMB AnaLev_0 (min,max,avg,range)= 2080    2094        2088        14
CSRTriggers_FailCode1=0      0  0  0  0  0  0  0
```

The ReadoutASICFIFO_FailCode is a 3 bit long integer number and it will be encountered from now on in any test that monitors the TBM digitized analog outputs.

Bit0= software type error

Bit1= error of ASIC Tester FIFO before digitizing (FIFO should be empty)

Bit2= error of ASIC Tester FIFO after digitizing (FIFO should be not empty and not full).

The CSRTriggers_FailCode1 is a 7 bit long integer number specific for this test. The SR1 status byte should be 0xA0 after all four triggers.

Bit0= error of ReadoutASICFIFO_FailCode

Bit1= error of SR1 status byte after triggering port 0

Bit2= error of SR1 status byte after triggering port 1

Bit3= error of SR1 status byte after triggering port 2

Bit4= error of SR1 status byte after triggering port 3

Bit5= error of TBMA response

Bit6= error of TBMB response

The TBMA and TBMB response should be a base line (no response) for all four triggers. To qualify that, the maximum and minimum values of all analog samples (calculated independently for each of the 4 triggers and 2 analog outputs) must fulfill the relation:

TBMX(max) - TBMX(min) < BaseLineMaxRange

Here the BaseLineMaxRange is a test program global variable that was set to 50 ADC counts for all the five wafers reported here.

The other data printed in blue color above (TBMA/B BaseLine, UltraBlack and AnaLev_0) are just extra information that is print out in accordance to some print flags that allows the report to be configured for as much detailed information is wanted.

T21SyncModeNormTrigg test description

The T21 test consists in following steps:

1. Set Sync mode (write 0x00 in registers E2, F2). Set the Normal (L1A) trigger type to be sent by the sequencer.
2. For each TBM port address 0,1,2,3 send one trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.

The test report looks like the following:

```
ReadoutASICFIFO_FailCode=0   0  0  0
TBMA BaseLine (min,max,avg,range)= 2030    2065        2045        35
TBMB BaseLine (min,max,avg,range)= 2030    2050        2039        20
TBMA UltraBlk (min,max,avg,range)= 978     1014        998         36
TBMB UltraBlk (min,max,avg,range)= 962     980         969         18
TBMA AnaLev_0 (min,max,avg,range)= 2011    2041        2025        30
TBMB AnaLev_0 (min,max,avg,range)= 2012    2027        2018        15
TBMA_AnalogLevels_FailCode(1)=0          0  0  0  0  0  0  0  0  0
TBMA_AnalogLevels_FailCode(2)=0          0  0  0  0  0  0  0  0  0
TBMA_AnalogLevels_FailCode(3)=0          0  0  0  0  0  0  0  0  0
TBMA_AnalogLevels_FailCode(4)=0          0  0  0  0  0  0  0  0  0
TBMB_AnalogLevels_FailCode(1)=0          0  0  0  0  0  0  0  0  0
TBMB_AnalogLevels_FailCode(2)=0          0  0  0  0  0  0  0  0  0
TBMB_AnalogLevels_FailCode(3)=0          0  0  0  0  0  0  0  0  0
TBMB_AnalogLevels_FailCode(4)=0          0  0  0  0  0  0  0  0  0
CSRTriggers_FailCode2=0      0  0  0  0  0
CSRTriggersTBMA_FailCode2=0  0  0  0  0  0  0  0  0  0  0
CSRTriggersTBMB_FailCode2=0  0  0  0  0  0  0  0  0  0  0
```

The ReadoutASICFIFO_FailCode was described previously.

The CSRTriggers_FailCode2 is a 5 bit long integer number specific for this test. The SR1 status byte should be 0xA3 after all four triggers.

Bit0= error of ReadoutASICFIFO_FailCode

Bit1= error of SR1 status byte after triggering port 0
Bit2= error of SR1 status byte after triggering port 1
Bit3= error of SR1 status byte after triggering port 2
Bit4= error of SR1 status byte after triggering port 3

The CSRTriggersTBMA_FailCode2 and CSRTriggersTBMA_FailCode2 are 10 bit long integer numbers. They monitor the TBMA and TBMB analog output response and will be encountered from now on in any test that monitors the TBM digitized analog outputs and verify the header and trailer bit settings.

Bit0= error of TBMA/B_AnalogLevels_FailCode (port 0 to 3)
Bit1= error of TBMA/B Header EventCounter number (port 0 to 3)
Bit2= error of TBMA/B Trailer NoTokenPass bit (port 0 to 3)
Bit3= error of TBMA/B Trailer TBMReset bit (port 0 to 3)
Bit4= error of TBMA/B Trailer ROCReset bit (port 0 to 3)
Bit5= error of TBMA/B Trailer SyncTrigError bit (port 0 to 3)
Bit6= error of TBMA/B Trailer SyncTrig bit (port 0 to 3)
Bit7= error of TBMA/B Trailer EventCounterCleared bit (port 0 to 3)
Bit8= error of TBMA/B Trailer PreCalibrateTrigger bit (port 0 to 3)
Bit9= error of TBMA/B Trailer StackFull bit (port 0 to 3)

The correct extraction of TBM Header and Trailer analog encoded bits from the digitized data is reflected in the so called TBMA/B_AnalogLevelsFailCode(1 to 4). The software algorithm for retrieving the analog levels consists in:

1. Calculate a BaseLine level by averaging before Header and after Trailer samples.
2. Check for the BaseLine to be within limits:
   BaseLine < BaseLineNominal + BaseLineMaxDev and
   BaseLine > BaseLineNominal – BaseLineMaxDev
   The BaseLineNominal and BaseLineMaxDev are test program global variables that were set to 2048 and 200 ADC counts respectively.
3. Calculate UltraBlack level by averaging Header and Trailer analog encoded bits.
4. Calculate Level_0 by averaging Header and Trailer analog encoded bits.
5. Calculate 9 theoretically equidistant AnalogLevel(), starting from the assumption that TBMA/B_AnalogStep = (Level_0 – UltraBlack) / 4
6. Check for each analog sample from the rest of TBM Header and Trailer to be found in one of the following accepted intervals
   Header/Trailer bit > AnalogLevel(i) - AnaWidth * TBMA/B_AnalogStep and
   Header/Trailer bit < AnalogLevel(i) + AnaWidth * TBMA/B_AnalogStep
   If any of the Header/Trailer bits is not within any of the accepted intervals, a flag error is set (for that specific bit) in the TBMA/B_AnalogLevelsFailCode(1 to 4) 9 bit long integer number.
7. Assign corresponding value to the decoded analog bit.

The AnaWidth is a global variables that was set to 0.4 (40%) for the five wafers reported here. It allows a variation of +-40% of any analog encoded bit w.r.t. the calculated theoretical value AnalogLevel(i), where i is from -4 to +4.

For this particular test, we look for the following Header and Trailer bit pattern:

	TBM A				TBM B			
	Port 0	Port 1	Port 2	Port 3	Port 0	Port 1	Port 2	Port 3
EventCounter	0	1	2	3	0	1	2	3
NoTokenPass	0	0	0	0	0	0	0	0
TBMReset	0	0	0	0	0	0	0	0
ROCReset	0	0	0	0	0	0	0	0
SyncTrigError	0	0	0	0	0	0	0	0
SyncTrig	0	0	0	0	0	0	0	0
EventCounterCleared	1	0	0	0	1	0	0	0
PreCalibrateTrigger	1	0	0	0	1	0	0	0
StackFull	0	0	0	0	0	0	0	0

T22SyncModeCSRTrigg test description

The T22 test consists in following steps:

1. Keep Sync mode. Set the CSR trigger type to be sent by the sequencer.
2. For each TBM port address 0,1,2,3 send one trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.

The test report and all fail codes are similar with the ones in T21. The SR1 status byte should be 0xA3 after all four triggers.

For this particular test, we look for the following Header and Trailer bit pattern:

	TBM A				TBM B			
	Port 0	Port 1	Port 2	Port 3	Port 0	Port 1	Port 2	Port 3
EventCounter	0	0	0	0	0	0	0	0
NoTokenPass	0	0	0	0	0	0	0	0
TBMReset	0	0	0	0	0	0	0	0
ROCReset	0	0	0	0	0	0	0	0
SyncTrigError	1	1	1	1	1	1	1	1
SyncTrig	1	1	1	1	1	1	1	1
EventCounterCleared	0	0	0	0	0	0	0	0
PreCalibrateTrigger	0	0	0	0	0	0	0	0
StackFull	0	0	0	0	0	0	0	0

T23ClearEventCounterModeNormTrigg test description

The T23 test consists in following steps:

1. Set ClearEventCounter mode. Set the Normal (L1A) trigger type to be sent by the sequencer.
2. For each TBM port address 0,1,2,3 send one trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.

The test report and all fail codes are similar with the ones in T22. The SR1 status byte should be 0xA3 after all four triggers.

For this particular test, we look for the following Header and Trailer bit pattern:

	TBM A				TBM B			
	Port 0	Port 1	Port 2	Port 3	Port 0	Port 1	Port 2	Port 3
EventCounter	1	2	3	4	1	2	3	4
NoTokenPass	0	0	0	0	0	0	0	0
TBMReset	0	0	0	0	0	0	0	0
ROCReset	0	0	0	0	0	0	0	0
SyncTrigError	0	0	0	0	0	0	0	0
SyncTrig	0	0	0	0	0	0	0	0
EventCounterCleared	0	0	0	0	0	0	0	0
PreCalibrateTrigger	0	0	0	0	0	0	0	0
StackFull	0	0	0	0	0	0	0	0

T24ClearEventCounterModeCSRNormTrigg test description

The T24 test consists in following steps:

1. Keep ClearEventCounter mode. Set the CSR trigger type to be sent by the sequencer. Send one trigger.
2. Set the Normal (L1A) trigger type to be sent by the sequencer.
3. For each TBM port address 0,1,2,3 send one trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.

The test report and all fail codes are similar with the ones in T23. The SR1 status byte should be 0xA3 after all four triggers.

For this particular test, we look for the following Header and Trailer bit pattern:

	TBM A				TBM B			
	Port 0	Port 1	Port 2	Port 3	Port 0	Port 1	Port 2	Port 3
EventCounter	0	1	2	3	0	1	2	3

NoTokenPass	0	0	0	0	0	0	0	0
TBMReset	0	0	0	0	0	0	0	0
ROCReset	0	0	0	0	0	0	0	0
SyncTrigError	0	0	0	0	0	0	0	0
SyncTrig	0	0	0	0	0	0	0	0
EventCounterCleared	1	0	0	0	1	0	0	0
PreCalibrateTrigger	0	0	0	0	0	0	0	0
StackFull	0	0	0	0	0	0	0	0

T25ClearEventCounterModeROCResetTrigg test description

The T25 test consists in following steps:

1. Keep ClearEventCounter mode. Set the ROCReset trigger type to be sent by the sequencer.
2. For each TBM port address 0,1,2,3 send one trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.

The test report and all fail codes are similar with the ones in T20. The SR1 status byte should be 0xA0 after all four triggers. We don't look for any Header and Trailer bit pattern - the analog output is checked to be a base line.

T26ClearEventCounterModeNormTrigg test description

The T26 test consists in following steps:

1. Keep ClearEventCounter mode. Set the Normal (L1A) trigger type to be sent by the sequencer.
2. For each TBM port address 0,1,2,3 send one trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.

The test report and all fail codes are similar with the ones in T24. The SR1 status byte should be 0xA3 after all four triggers.

For this particular test, we look for the following Header and Trailer bit pattern:

	TBM A				TBM B			
	Port 0	Port 1	Port 2	Port 3	Port 0	Port 1	Port 2	Port 3
EventCounter	4	5	6	7	4	5	6	7
NoTokenPass	0	0	0	0	0	0	0	0
TBMReset	0	0	0	0	0	0	0	0
ROCReset	1	0	0	0	1	0	0	0

SyncTrigError	0	0	0	0	0	0	0	0
SyncTrig	0	0	0	0	0	0	0	0
EventCounterCleared	0	0	0	0	0	0	0	0
PreCalibrateTrigger	0	0	0	0	0	0	0	0
StackFull	0	0	0	0	0	0	0	0

T27ClearEventCounterModeTBMResetTrigg test description

The T27 test consists in following steps:

1. Keep ClearEventCounter mode. Set the TBMReset trigger type to be sent by the sequencer.
2. For each TBM port address 0,1,2,3 send one trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.

The test report and all fail codes are similar with the ones in T25. The SR1 status byte should be 0xA0 after all four triggers. We don't look for any Header and Trailer bit pattern - the analog output is checked to be a base line.

T28ClearEventCounterModeNormTrigg test description

The T28 test consists in following steps:

1. Keep ClearEventCounter mode. Set the Normal (L1A) trigger type to be sent by the sequencer.
2. For each TBM port address 0,1,2,3 send one trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.

The test report and all fail codes are similar with the ones in T26. The SR1 status byte should be 0xA3 after all four triggers.

For this particular test, we look for the following Header and Trailer bit pattern:

	TBM A				TBM B			
	Port 0	Port 1	Port 2	Port 3	Port 0	Port 1	Port 2	Port 3
EventCounter	1	2	3	4	1	2	3	4
NoTokenPass	0	0	0	0	0	0	0	0
TBMReset	1	0	0	0	1	0	0	0
ROCReset	1	0	0	0	1	0	0	0
SyncTrigError	0	0	0	0	0	0	0	0
SyncTrig	0	0	0	0	0	0	0	0
EventCounterCleared	0	0	0	0	0	0	0	0

PreCalibrateTrigger	0	0	0	0	0	0	0	0
StackFull	0	0	0	0	0	0	0	0

T29ReadoutMode20MHz test description

The T29 test consists in following steps:

1. Set Calibrate mode. Set the Normal (L1A) trigger type to be sent by the sequencer. Set the 20MHz Readout speed.
2. For each TBM port address 0,1,2,3 send one trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.
3. Set back the 40MHz Readout speed.

The test report and all fail codes are similar with the ones in T28. The SR1 status byte should be 0xA3 after all four triggers.

For this particular test, we look for the following Header and Trailer bit pattern:

	TBM A				TBM B			
	Port 0	Port 1	Port 2	Port 3	Port 0	Port 1	Port 2	Port 3
EventCounter	5	6	7	8	5	6	7	8
NoTokenPass	0	0	0	0	0	0	0	0
TBMReset	0	0	0	0	0	0	0	0
ROCReset	0	0	0	0	0	0	0	0
SyncTrigError	0	0	0	0	0	0	0	0
SyncTrig	0	0	0	0	0	0	0	0
EventCounterCleared	0	0	0	0	0	0	0	0
PreCalibrateTrigger	0	0	0	0	0	0	0	0
StackFull	0	0	0	0	0	0	0	0

T31TBMStack32NormTrigg test description

The T31 test consists in following steps:

1. Do a chip reset. Set TokenOut connected to TokenIn on both TBMs. Send one TBMReset trigger. Set 40MHz ReadoutSpeed. Set PauseReadout bit on both TBMs (write 0x09 in registers E0, F0).
2. Send 32 L1A triggers. Monitor ONLY the SR1 status byte after triggering port 0, 1, 2 and 3 and then again the same ports, up to 8 times (8*4=32).

There is one fail code number associated with this test:
Bit0= software type error
Bit1= error if any of the first 14 L1A triggers produce a status register SR1<>0xA0

Bit2= error if any of the last 18 L1A triggers produce a status register SR1<>0x80

T32TBMStack32StackCount test description

The T32 test consists in following steps:
1. Set the StackReadBackMode bit (write 0x19 in registers E0, F0).
2. Read the number of items (events) on stack (write 0xFF in registers E3, F3).

There is one fail code number associated with this test:
Bit0= software type error
Bit1= error if the number of items (events) on TBMA stack is not 0x20=32decimal
Bit2= error if the number of items (events) on TBMB stack is not 0x20=32decimal

T33TBMStack32StackEvent test description

The T33 test consists in following steps:
1. Verify stack content by reading Stack Status bits D15 to D08 (write 0xFF in registers E7, F7).
2. Verify stack content by reading Stack Event Number bits D07 to D00 (write 0xFF in registers E5, F5).
3. Repeat steps 1 and 2 for 36 times (minimum is 32 and have 4 extra readings)

There is one fail code number associated with this test:
Bit0= software type error
Bit1= error on Stack Status bits D15 to D08 on TBMA
Bit2= error on Stack Status bits D15 to D08 on TBMB
Bit3= error on Stack Event Number bits D07 to D00 on TBMA
Bit4= error on Stack Event Number bits D07 to D00 on TBMB

The Stack Status bits D15 to D08 and Stack Event Number bits D07 to D00 for TBMA and TBMB should obey the following pattern:

	Status bits D15 to D08		Stack Event Number bits D07 to D00	
	TBMA	TBMB	TBMA	TBMB
I=1	0x60	0x60	I	I
I=2 to 14	0x00	0x00	I	I
I=15 to 32	0x80	0x80	I	I
I=33	0x60	0x60	I-32	I-32
I=34 to 36	0x00	0x00	I-32	I-32

T34TBMStack32ReadVerify test description

The T34 test consists in following steps:

1. Clear StackReadBackMode bit and PauseReadout bit (write 0x01 in registers E0, F0).
2. Send 36 L1A triggers. Monitor response for port 0, 1, 2 and 3 and then again the same ports, up to 9 times (9*4=36). The monitoring includes the interface board status register SR1 and the TBM analog output digitization.

The test report looks like the following:

ReadoutASICFIFO_FailCode=0 0 0 0
TBMA BaseLine (min,max,avg,range)= 2025 2064 2042 39
TBMB BaseLine (min,max,avg,range)= 2028 2055 2039 27
TBMA UltraBlk (min,max,avg,range)= 972 1014 994 42
TBMB UltraBlk (min,max,avg,range)= 950 987 965 37
TBMA AnaLev_0 (min,max,avg,range)= 2004 2041 2024 37
TBMB AnaLev_0 (min,max,avg,range)= 2010 2030 2019 20
TBMA_AnalogLevels_FailCode(1)=0 0 0 0 0 0 0 0 0 0
TBMA_AnalogLevels_FailCode(2)=0 0 0 0 0 0 0 0 0 0
.....
TBMA_AnalogLevels_FailCode(35)=0 0 0 0 0 0 0 0 0 0
TBMA_AnalogLevels_FailCode(36)=0 0 0 0 0 0 0 0 0 0
TBMB_AnalogLevels_FailCode(1)=0 0 0 0 0 0 0 0 0 0
TBMB_AnalogLevels_FailCode(2)=0 0 0 0 0 0 0 0 0 0
.....
TBMB_AnalogLevels_FailCode(35)=0 0 0 0 0 0 0 0 0 0
TBMB_AnalogLevels_FailCode(36)=0 0 0 0 0 0 0 0 0 0
TBMStack32_FailCode4=0 0 0
TBMStack32TBMA_FailCode4=0 0 0 0 0 0 0 0 0 0 0
TBMStack32TBMB_FailCode4=0 0 0 0 0 0 0 0 0 0 0

The fail codes are similar with the ones in T29 except the TBMStack32_FailCode4 has only two bits. The SR1 status byte should be 0xA3 after all 36 triggers.

Bit0= error of ReadoutASICFIFO_FailCode

Bit1= error of SR1 status byte after any of the 36 triggers

For this particular test, we look for the following Header and Trailer bit pattern:

	TBMA		TBMB	
	for I=1	for I>1	for I=1	for I>1
EventCounter	I+32	I+32	I+32	I+32
NoTokenPass	0	0	0	0
TBMReset	0	0	0	0
ROCReset	0	0	0	0
SyncTrigError	0	0	0	0

SyncTrig	0	0	0	0
EventCounterCleared	0	0	0	0
PreCalibrateTrigger	0	0	0	0
StackFull	1	0	1	0

T35TBMStack24NormTrigg test description

The T35 test consists in following steps:

1. Set StackFullOnCount24 bit and also set PauseReadout bit on both TBMs (write 0x0D in registers E0, F0).
2. Send 32 L1A triggers. Monitor ONLY the SR1 status byte after triggering port 0, 1, 2 and 3 and then again the same ports, up to 8 times (8*4=32).

There is one fail code number associated with this test:
Bit0= software type error
Bit1= error if any of the first 14 L1A triggers produce a status register SR1<>0xA0
Bit2= error if any of the last 18 L1A triggers produce a status register SR1<>0x80

T36TBMStack24ReadVerify test description

The T36 test consists in following steps:

1. Clear PauseReadout bit (write 0x05 in registers E0, F0).
2. Send 28 L1A triggers. Monitor response for port 0, 1, 2 and 3 and then again the same ports, up to 7 times (7*4=28). The monitoring includes the interface board status register SR1 and the TBM analog output digitization.
3. Disconnect TokenOut from TokenIn on both TBMs. Do a chip reset. Set 40MHz ReadoutSpeed.

The test report looks like on T34 test, except the TBMA/B_AnalogLevels_FailCode array index goes up to only 28 instead of 36.

The fail codes are similar with the ones in T34. The SR1 status byte should be 0xA3 after all 28 triggers.

For this particular test, we look for the following Header and Trailer bit pattern:

	TBMA		TBMB	
	I=1	I>1	I=1	I>1
EventCounter	I+100	I+100	I+100	I+100
NoTokenPass	0	0	0	0
TBMReset	0	0	0	0
ROCReset	0	0	0	0

SyncTrigError	0	0	0	0
SyncTrig	0	0	0	0
EventCounterCleared	0	0	0	0
PreCalibrateTrigger	0	0	0	0
StackFull	1	0	1	0

T41ScanRegAnaInpBias test description

The T41 test consists in following steps:

1. Set DisableTriggerOut bit for both TBMs (write 0x41 in registers E0, F0). Disable TokenIn bit for both TBMs. Set positive pulse amplitude to 0x0A00 (~0.417V), on port 0.
2. Scan the AnalogInputBias register EA using hex values=0x40, 0x80 and 0xC0. Send one Normal (L1A) trigger. Monitor response (only for port 0) after each setting. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.
3. Reset the AnalogInputBias to default 0x80.

Note that, for all the following tests that include external pulse amplitude settings, the pulse voltage listed is basically applied to a voltage divider made from a 750 ohms resistor in series with the TBM input resistance.

The test report looks like the following:

AnalogInputBias Register Test Report
ReadoutASICFIFO_FailCode=0 0 0 0
TBMA BaseLine (min,max,avg,range)= 2163 2165 2164 2
TBMB BaseLine (min,max,avg,range)= 2038 2041 2039 3
TBMA UltraBlk (min,max,avg,range)= 1076 1080 1078 4
TBMB UltraBlk (min,max,avg,range)= 1097 1100 1099 3
TBMA AnaLev_0 (min,max,avg,range)= 2028 2036 2031 8
TBMB AnaLev_0 (min,max,avg,range)= 2021 2023 2022 2
TBMA_AnalogLevels_FailCode(1)=0 0 0 0 0 0 0 0 0 0
TBMA_AnalogLevels_FailCode(2)=0 0 0 0 0 0 0 0 0 0
TBMA_AnalogLevels_FailCode(3)=0 0 0 0 0 0 0 0 0 0
TBMB_AnalogLevels_FailCode(1)=0 0 0 0 0 0 0 0 0 0
TBMB_AnalogLevels_FailCode(2)=0 0 0 0 0 0 0 0 0 0
TBMB_AnalogLevels_FailCode(3)=0 0 0 0 0 0 0 0 0 0
TBMAnalogOutput_FailCode1=0 0 0 0 0
TBMAnalogOutputTBMA_FailCode1=0 0 0 0 0 0 0 0 0 0 0
TBMAnalogOutputTBMB_FailCode1=0 0 0 0 0 0 0 0 0 0 0

The TBMAnalogOutput_FailCode1 is a 4 bit long integer number with the following significance:

Bit0= error of ReadoutASICFIFO_FailCode

Bit1= error of SR1 status byte after first register writing or after sending the trigger
Bit2= error of SR1 status byte after second register writing or after sending the trigger
Bit3= error of SR1 status byte after third register writing or after sending the trigger

The SR1 status byte should be, for all 3 scan values, 0x90 after register writing and 0x80 after sending the trigger.

For this particular test, we look for the following Header and Trailer bit pattern:

	TBMA			TBMB		
	Val=0x40	Val=0x80	Val=0xC0	Val=0x40	Val=0x80	Val=0xC0
EventCounter	1	2	3	1	2	3
NoTokenPass	1	1	1	1	1	1
TBMReset	0	0	0	0	0	0
ROCReset	0	0	0	0	0	0
SyncTrigError	0	0	0	0	0	0
SyncTrig	0	0	0	0	0	0
EventCounterCleared	0	0	0	0	0	0
PreCalibrateTrigger	0	0	0	0	0	0
StackFull	0	0	0	0	0	0

T42ScanRegAnaOutBias test description

The T42 test consists in following steps:
1. Keep previous settings.
2. Scan the AnalogOutputBias register EC using hex values=0x40, 0x80 and 0xC0. Send one Normal (L1A) trigger. Monitor response (only for port 0) after each setting. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.
3. Reset the AnalogOutputBias to default 0x80.

The test report and all fail codes are similar with the ones in T41. The SR1 status byte should be, for all 3 scan values, 0x90 after register writing and 0x80 after sending the trigger.

For this particular test, we look for the following Header and Trailer bit pattern:

	TBMA			TBMB		
	Val=0x40	Val=0x80	Val=0xC0	Val=0x40	Val=0x80	Val=0xC0
EventCounter	4	5	6	4	5	6
NoTokenPass	1	1	1	1	1	1
TBMReset	0	0	0	0	0	0
ROCReset	0	0	0	0	0	0
SyncTrigError	0	0	0	0	0	0
SyncTrig	0	0	0	0	0	0

EventCounterCleared	0	0	0	0	0	0
PreCalibrateTrigger	0	0	0	0	0	0
StackFull	0	0	0	0	0	0

T43ScanRegAnaOutGain test description

The T43 test consists in following steps:

1. Keep previous settings.
2. Scan the AnalogOutputGain register EE using hex values=0x40, 0x80 and 0xC0. Send one Normal (L1A) trigger. Monitor response (only for port 0) after each setting. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.
3. Reset the AnalogOutputGain to default 0x80.
4. Reset DisableTriggerOut bit for both TBMs (write 0x01 in registers E0, F0). Re-enable TokenIn bit for both TBMs.

The test report and all fail codes are similar with the ones in T42. The SR1 status byte should be, for all 3 scan values, 0x90 after register writing and 0x80 after sending the trigger.

For this particular test, we look for the following Header and Trailer bit pattern:

	TBMA			TBMB		
	Val=0x40	Val=0x80	Val=0xC0	Val=0x40	Val=0x80	Val=0xC0
EventCounter	7	8	9	7	8	9
NoTokenPass	1	1	1	1	1	1
TBMReset	0	0	0	0	0	0
ROCReset	0	0	0	0	0	0
SyncTrigError	0	0	0	0	0	0
SyncTrig	0	0	0	0	0	0
EventCounterCleared	0	0	0	0	0	0
PreCalibrateTrigger	0	0	0	0	0	0
StackFull	0	0	0	0	0	0

***T44RiseFallTimesP0* test description**

The T44 test consists in following steps:

1. Measure the RisingEdge and FallingEdge of UltraBlack and Pulse signals applied at TBMA port 0 (positive pulse, fixed Pulse amplitude 0x0A00~0.391Volts). Scan the ADC converter clock delay in 10 steps of 2.5ns delay (40MHz clock)

The test report looks like the following:
TBMA Port0 Positive Pulse Injection Test Report

ReadoutASICFIFO_FailCode=0 0 0 0
TBMTransient_FailCode1=0
TBMA_UBRE=6.05ns 1407 1649
TBMA_UBFE=6.17ns 4412 4659
TBMB_UBRE=6.6ns 1345 1609
TBMB_UBFE=6.82ns 4349 4622
TBMA_PULSERE=9.72ns 2645 3034
TBMA_PULSEFE=10.42ns 3628 4045

The fail code associated with this test has only one bit, which is set if there is any failure of type ReadoutASICFIFO_FailCode. There is no SR1 status byte check and no other failure check associated with TBM Header and Trailer bit pattern.

The Ultra Black rising and falling edge for both TBMs together with the rising and falling edge for the Pulse signal associated to the specific port are calculated using the following algorithm:

1. Calculate the average value of the base line over 10 measurements. Subtract it from the measured signal and take absolute value. Find maximum and normalize data to this maximum. The rising edge and falling edge times will be associated to this normalized, always positive signal.
2. Find adjacent (time) indexes where signal is crossing 10% and then 90%. Interpolate between the adjacent indexes and round the new (non integer) index to 0.01. Take the difference between the (new) interpolated indexes for 10% and 90% and multiply it with the 2.5ns step value and keep only two decimals. This is the rise or fall time reported above, with a precision of 0.025ns before rounding to two decimals.

T45RiseFallTimesP1 **test description**

The T45 test consists in following steps:

1. Measure the RisingEdge and FallingEdge of UltraBlack and Pulse signals applied at TBMA port 1 (negative pulse, fixed Pulse amplitude 0x0A00~0.391Volts). Scan the ADC converter clock delay in 10 steps of 2.5ns delay (40MHz clock)

The test report looks like the following:

TBMA Port1 Negative Pulse Injection Test Report
ReadoutASICFIFO_FailCode=0 0 0 0
TBMTransient_FailCode1=0
TBMA_UBRE=6.1ns 1347 1591
TBMA_UBFE=6.25ns 4349 4599
TBMB_UBRE=6.62ns 1344 1609
TBMB_UBFE=6.9ns 4340 4616
TBMA_PULSERE=10.17ns 2642 3049
TBMA_PULSEFE=10.2ns 3633 4041

T46RiseFallTimesP2 test description

The T46 test consists in following steps:

1. Measure the RisingEdge and FallingEdge of UltraBlack and Pulse signals applied at TBMB port 2 (positive pulse, fixed Pulse amplitude 0x0A00~0.391Volts).
2. Scan the ADC converter clock delay in 10 steps of 2.5ns delay (40MHz clock)

The test report looks like the following:

TBMB Port2 Positive Pulse Injection Test Report
ReadoutASICFIFO_FailCode=0 0 0 0
TBMTransient_FailCode1=0
TBMA_UBRE=5.95ns 1351 1589
TBMA_UBFE=6.2ns 4354 4602
TBMB_UBRE=6.32ns 1345 1598
TBMB_UBFE=7.02ns 4342 4623
TBMB_PULSERE=10.45ns 2649 3067
TBMB_PULSEFE=11.45ns 3647 4105

T47RiseFallTimesP3 test description

The T47 test consists in following steps:

1. Measure the RisingEdge and FallingEdge of UltraBlack and Pulse signals applied at TBMB port 3 (negative pulse, fixed Pulse amplitude 0x0A00~0.391Volts). Scan the ADC converter clock delay in 10 steps of 2.5ns delay (40MHz clock)

The test report looks like the following:

TBMB Port3 Negative Pulse Injection Test Report
ReadoutASICFIFO_FailCode=0 0 0 0
TBMTransient_FailCode1=0
TBMA_UBRE=5.82ns 1351 1584
TBMA_UBFE=6.25ns 4354 4604
TBMB_UBRE=6.37ns 1404 1659
TBMB_UBFE=6.45ns 4407 4665
TBMB_PULSERE=11.02ns 2650 3091
TBMB_PULSEFE=10.92ns 3654 4091

T48PulseLinP0 test description

The T48 test consists in following steps:

1. Measure the linearity response of TBMA port 0 when the Pulse signal amplitude goes from negative 0x2000 to positive 0x2000 (-1.25V to +1.25V) in 16 steps of 0x0400 (0.15625V)

The test report looks like the following:

```
************************************************************
TBM Linearity Pulse Test Report
ReadoutASICFIFO_FailCode=0   0  0  0
600 663 767 913 1060 1201 1437 1702 1992 2266 2510 2748 2936 3066 3187 3267 3288
TBMLinearity_FailCode=0      0  0  0
ReadoutASICFIFO_FailCode=0   0  0  0
730 796 911 997 1141 1313 1520 1777 2025 2274 2503 2693 2878 3015 3072 3199 3291
TBMLinearity_FailCode=0      0  0  0
************************************************************
```

There is one fail code number associated with this test:
Bit0= error of ReadoutASICFIFO_FailCode
Bit1= error in finding TBMB response as a base line when Pulse injected on TBMA
Bit2= error in finding TBMA response as a base line when Pulse injected on TBMB

The SR1 status byte is not checked. Instead the TBM to which is NOT applied the pulse is checked to be a base line (no output) in a similar way as it was done it T20 and T21, using the formula:

Abs(Measurement - BaseLineNominal) >= BaseLineMaxDev + BaseLineMaxRange / 2
Abs(Measurement - BaseLineNominal) <= BaseLineMaxDev - BaseLineMaxRange / 2

The BaseLineNominal and BaseLineMaxDev and BaseLineMaxRange are test program global variables that were set to 2048, 200 and 50 ADC counts respectively. There is no linear interpolation of measured data.

T49PulseLinP2 **test description**

The T49 test consists in following steps:

1. Measure the linearity response of TBMB port 2 when the Pulse signal amplitude goes from negative 0x2000 to positive 0x2000 (-1.25V to +1.25V) in 16 steps of 0x0400 (0.15625V)

The test report and all fail codes are similar with the ones in T48.

T51SingleTBMA test description

The first part of T51 test consists in following steps:

1. Reset TBM. Shutdown TBM B Clock (write 0x01 in registers E0 and 0x03 in register F0). Set the Normal (L1A) trigger type to be sent by the sequencer.
2. For each TBM port address 0,1,2,3 send one trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.

The test report looks like the following:

```
ReadoutASICFIFO_FailCode=0   0  0  0
TBMA BaseLine (min,max,avg,range)= 1999    2003        2002        4
TBMB BaseLine (min,max,avg,range)= 2018    2020        2019        2
TBMA UltraBlk (min,max,avg,range)= 1069    1084        1077        15
TBMB UltraBlk (min,max,avg,range)= 2013    2015        2014        2
TBMA AnaLev_0 (min,max,avg,range)= 1986    1990        1988        4
TBMB AnaLev_0 (min,max,avg,range)= 2020    2026        2023        6
TBMA_AnalogLevels_FailCode1(1)=0         0  0  0  0  0  0  0  0  0
TBMA_AnalogLevels_FailCode1(2)=0         0  0  0  0  0  0  0  0  0
TBMA_AnalogLevels_FailCode1(3)=0         0  0  0  0  0  0  0  0  0
TBMA_AnalogLevels_FailCode1(4)=0         0  0  0  0  0  0  0  0  0
SingleTBMA_FailCode1=0      0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0
```

The SingleTBMA_FailCode1 is a 16 bit long integer number:
Bit0= error of ReadoutASICFIFO_FailCode
Bit1= error of SR1 status byte after triggering port 0 (not equal with "A1")
Bit2= error of SR1 status byte after triggering port 1 (not equal with "A1")
Bit3= error of SR1 status byte after triggering port 2 (not equal with "01")
Bit4= error of SR1 status byte after triggering port 3 (not equal with "01")
Bit5= error of TBMA_AnalogLevels_FailCode (port 0 to 3)
Bit6= error of TBMA Header EventCounter number (port 0 to 3)
Bit7= error of TBMA Trailer NoTokenPass bit (port 0 to 3)
Bit8= error of TBMA Trailer TBMReset bit (port 0 to 3)
Bit9= error of TBMA Trailer ROCReset bit (port 0 to 3)
Bit10= error of TBMA Trailer SyncTrigError bit (port 0 to 3)
Bit11= error of TBMA Trailer SyncTrig bit (port 0 to 3)
Bit12= error of TBMA Trailer EventCounterCleared bit (port 0 to 3)
Bit13= error of TBMA Trailer PreCalibrateTrigger bit (port 0 to 3)
Bit14= error of TBMA Trailer StackFull bit (port 0 to 3)
Bit15= error of TBMB response is not a base line

For this particular test, we look for the following Header and Trailer bit pattern:

	TBM A			
	Port 0	Port 1	Port 2	Port 3
EventCounter	1	2	3	4

NoTokenPass	0	0	0	0
TBMReset	0	0	0	0
ROCReset	0	0	0	0
SyncTrigError	0	0	0	0
SyncTrig	0	0	0	0
EventCounterCleared	0	0	0	0
PreCalibrateTrigger	0	0	0	0
StackFull	0	0	0	0

T51SingleTBMAOnly test description

The second part of T51 test consists in following steps:

1. Switch to TBM A only. Use TBM B control register to disable TokenOut and AnalogOut drivers (write 0x03 in registers F8).
2. For each TBM port address 0,1,2,3 send one trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.
3. Re-enable TBM B Clock (write 0x01 in register F0). Re-enable TokenOut and AnalogOut drivers (write 0x00 in registers F8).

The test report and the fail code are similar with the ones in T51 part 1. The SR1 status byte should be 0xA3 after all four triggers.

For this particular test, we look for the following Header and Trailer bit pattern:

	TBM A			
	Port 0	Port 1	Port 2	Port 3
EventCounter	5	6	7	8
NoTokenPass	0	0	0	0
TBMReset	0	0	0	0
ROCReset	0	0	0	0
SyncTrigError	0	0	0	0
SyncTrig	0	0	0	0
EventCounterCleared	0	0	0	0
PreCalibrateTrigger	0	0	0	0
StackFull	0	0	0	0

T52SingleTBMB test description

The first part of T52 test consists in following steps:

1. Reset TBM. Shutdown TBM A Clock (write 0x03 in registers E0 and 0x01 in register F0). Set the Normal (L1A) trigger type to be sent by the sequencer.

2. For each TBM port address 0,1,2,3 send one trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.

The test report looks like the following:

```
ReadoutASICFIFO_FailCode=0   0  0  0
TBMA BaseLine (min,max,avg,range)= 2003    2006        2004        3
TBMB BaseLine (min,max,avg,range)= 2015    2016        2016        1
TBMA UltraBlk (min,max,avg,range)= 1999    2001        2000        2
TBMB UltraBlk (min,max,avg,range)= 1094    1110        1101        16
TBMA AnaLev_0 (min,max,avg,range)= 2008    2011        2010        3
TBMB AnaLev_0 (min,max,avg,range)= 1993    1999        1997        6
TBMB_AnalogLevels_FailCode1(1)=0          0  0  0  0  0  0  0  0  0
TBMB_AnalogLevels_FailCode1(2)=0          0  0  0  0  0  0  0  0  0
TBMB_AnalogLevels_FailCode1(3)=0          0  0  0  0  0  0  0  0  0
TBMB_AnalogLevels_FailCode1(4)=0          0  0  0  0  0  0  0  0  0
SingleTBMB_FailCode1=0      0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0
```

The SingleTBMB_FailCode1 is a 16 bit long integer number:
Bit0= error of ReadoutASICFIFO_FailCode
Bit1= error of SR1 status byte after triggering port 0 (not equal with "02")
Bit2= error of SR1 status byte after triggering port 1 (not equal with "02")
Bit3= error of SR1 status byte after triggering port 2 (not equal with "A2")
Bit4= error of SR1 status byte after triggering port 3 (not equal with "A2")
Bit5= error of TBMB_AnalogLevels_FailCode (port 0 to 3)
Bit6= error of TBMB Header EventCounter number (port 0 to 3)
Bit7= error of TBMB Trailer NoTokenPass bit (port 0 to 3)
Bit8= error of TBMB Trailer TBMReset bit (port 0 to 3)
Bit9= error of TBMB Trailer ROCReset bit (port 0 to 3)
Bit10= error of TBMB Trailer SyncTrigError bit (port 0 to 3)
Bit11= error of TBMB Trailer SyncTrig bit (port 0 to 3)
Bit12= error of TBMB Trailer EventCounterCleared bit (port 0 to 3)
Bit13= error of TBMB Trailer PreCalibrateTrigger bit (port 0 to 3)
Bit14= error of TBMB Trailer StackFull bit (port 0 to 3)
Bit15= error of TBMA response is not a base line

For this particular test, we look for the following Header and Trailer bit pattern:

	TBM B			
	Port 0	Port 1	Port 2	Port 3
EventCounter	1	2	3	4
NoTokenPass	0	0	0	0
TBMReset	0	0	0	0
ROCReset	0	0	0	0
SyncTrigError	0	0	0	0
SyncTrig	0	0	0	0

EventCounterCleared	0	0	0	0
PreCalibrateTrigger	0	0	0	0
StackFull	0	0	0	0

T52SingleTBMBOnly test description

The second part of T52 test consists in following steps:

1. Switch to TBM B only. Use TBM A control register to disable TokenOut and AnalogOut drivers (write 0x03 in registers E8).
2. For each TBM port address 0,1,2,3 send one trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.
3. Re-enable TBM A Clock (write 0x01 in register E0). Re-enable TokenOut and AnalogOut drivers (write 0x00 in registers E8).

The test report and the fail code are similar with the ones in T52 part 1. The SR1 status byte should be 0xA3 after all four triggers.

For this particular test, we look for the following Header and Trailer bit pattern:

	TBM B			
	Port 0	Port 1	Port 2	Port 3
EventCounter	5	6	7	8
NoTokenPass	0	0	0	0
TBMReset	0	0	0	0
ROCReset	0	0	0	0
SyncTrigError	0	0	0	0
SyncTrig	0	0	0	0
EventCounterCleared	0	0	0	0
PreCalibrateTrigger	0	0	0	0
StackFull	0	0	0	0

T61IgnoreIncommTrigg test description

The T61 test consists in following steps:

1. Set the TBMReset trigger type to be sent by the sequencer. Send one trigger.
2. Set IgnoreIncomingTriggers bit (write 0x11 in registers E0, F0). Set the Normal (L1A) trigger type to be sent by the sequencer.
3. For each TBM port address 0,1,2,3 send one trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.
4. Reset IgnoreIncomingTriggers bit (write 0x01 in registers E0, F0).

The test report looks like the following:

```
************************************************************
BothTBMs - IgnoreIncomingTriggers Test Report
ReadoutASICFIFO_FailCode=0   0  0  0
TBMA BaseLine (min,max,avg,range)= 2003    2004        2004        1
TBMB BaseLine (min,max,avg,range)= 2017    2019        2018        2
TBMA UltraBlk (min,max,avg,range)= 2002    2005        2003        3
TBMB UltraBlk (min,max,avg,range)= 2016    2020        2017        4
TBMA AnaLev_0 (min,max,avg,range)= 2002    2004        2003        2
TBMB AnaLev_0 (min,max,avg,range)= 2017    2019        2018        2
IgnoreIncomingTriggers_FailCode=0        0  0  0  0  0  0  0
************************************************************
```

The IgnoreIncomingTriggers_FailCode is a 7 bit long integer number similar with the one in T20. The SR1 status byte should be 0x80 after all four triggers.

Bit0= error of ReadoutASICFIFO_FailCode
Bit1= error of SR1 status byte after triggering port 0
Bit2= error of SR1 status byte after triggering port 1
Bit3= error of SR1 status byte after triggering port 2
Bit4= error of SR1 status byte after triggering port 3
Bit5= error of TBMA response
Bit6= error of TBMB response

The TBMA and TBMB response should be a base line (no response) for all four triggers. To qualify that the same condition as in T20 is used.

T62DisableTrigg test description

The T62 test consists in following steps:

1. Set DisableTriggerOut bit (write 0x41 in registers E0, F0). Set the Normal (L1A) trigger type to be sent by the sequencer.
2. For each TBM port address 0,1,2,3 send one trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.
3. Reset DisableTriggerOut bit (write 0x01 in registers E0, F0).

The test report looks like the following:

```
************************************************************
BothTBMs - DisableTriggers Test Report
ReadoutASICFIFO_FailCode=0   0  0  0
TBMA BaseLine (min,max,avg,range)= 2001    2004        2002        3
TBMB BaseLine (min,max,avg,range)= 2015    2018        2016        3
TBMA UltraBlk (min,max,avg,range)= 1065    1105        1084        40
```

```
TBMB UltraBlk (min,max,avg,range)= 1080    1120        1099        40
TBMA AnaLev_0 (min,max,avg,range)= 1988    1991        1990        3
TBMB AnaLev_0 (min,max,avg,range)= 2000    2002        2001        2
TBMA_AnalogLevels_FailCode(1)=0          0 0 0 0 0 0 0 0 0
TBMA_AnalogLevels_FailCode(2)=0          0 0 0 0 0 0 0 0 0
TBMA_AnalogLevels_FailCode(3)=0          0 0 0 0 0 0 0 0 0
TBMA_AnalogLevels_FailCode(4)=0          0 0 0 0 0 0 0 0 0
TBMB_AnalogLevels_FailCode(1)=0          0 0 0 0 0 0 0 0 0
TBMB_AnalogLevels_FailCode(2)=0          0 0 0 0 0 0 0 0 0
TBMB_AnalogLevels_FailCode(3)=0          0 0 0 0 0 0 0 0 0
TBMB_AnalogLevels_FailCode(4)=0          0 0 0 0 0 0 0 0 0
DisableTriggers_FailCode=0   0 0 0 0 0
DisableTriggersTBMA_FailCode=0          0 0 0 0 0 0 0 0 0 0
DisableTriggersTBMB_FailCode=0          0 0 0 0 0 0 0 0 0 0
************************************************************
```

The test report and all fail codes are similar with the ones in T21. The SR1 status byte should be 0x80 after all four triggers.

For this particular test, we look for the following Header and Trailer bit pattern:

	TBM A				TBM B			
	Port 0	Port 1	Port 2	Port 3	Port 0	Port 1	Port 2	Port 3
EventCounter	1	2	3	4	1	2	3	4
NoTokenPass	1	1	1	1	1	1	1	1
TBMReset	1	0	0	0	1	0	0	0
ROCReset	1	0	0	0	1	0	0	0
SyncTrigError	0	0	0	0	0	0	0	0
SyncTrig	0	0	0	0	0	0	0	0
EventCounterCleared	0	0	0	0	0	0	0	0
PreCalibrateTrigger	0	0	0	0	0	0	0	0
StackFull	0	0	0	0	0	0	0	0

T67InjectROCResetTriggTBMA test description

The T67 test consists in following steps:

1. Set TokenOut connected to TokenIn on both TBMs. Set Normal (L1A) trigger type to be sent by the sequencer.
2. For each TBM port address 0,1,2,3 set InjectROCResetTrigger bit for TBMA (write 0x04 in registers E4). Send one L1A trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.

The test report and all fail codes are similar with the ones in T62. The SR1 status byte should be 0xB0, 0xB0, 0x90 and 0x90 after each set of InjectROCResetTrigger bit. The SR1 status byte should be 0xA3 after all four triggers.

For this particular test, we look for the following Header and Trailer bit pattern:

	TBM A				TBM B			
	Port 0	Port 1	Port 2	Port 3	Port 0	Port 1	Port 2	Port 3
EventCounter	5	6	7	8	5	6	7	8
NoTokenPass	0	0	0	0	0	0	0	0
TBMReset	0	0	0	0	0	0	0	0
ROCReset	1	1	1	1	0	0	0	0
SyncTrigError	0	0	0	0	0	0	0	0
SyncTrig	0	0	0	0	0	0	0	0
EventCounterCleared	0	0	0	0	0	0	0	0
PreCalibrateTrigger	0	0	0	0	0	0	0	0
StackFull	0	0	0	0	0	0	0	0

T68InjectROCResetTriggTBMB test description

The T68 test consists in following steps:

1. For each TBM port address 0,1,2,3 set InjectROCResetTrigger bit for TBMB (write 0x04 in registers F4). Send one L1A trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.

The test report and all fail codes are similar with the ones in T67. The SR1 status byte should be 0x90, 0x90, 0xB0, 0xB0 after each set of InjectROCResetTrigger bit. The SR1 status byte should be 0xA3 after all four triggers.

For this particular test, we look for the following Header and Trailer bit pattern:

	TBM A				TBM B			
	Port 0	Port 1	Port 2	Port 3	Port 0	Port 1	Port 2	Port 3
EventCounter	9	10	11	12	9	10	11	12
NoTokenPass	0	0	0	0	0	0	0	0
TBMReset	0	0	0	0	0	0	0	0
ROCReset	0	0	0	0	1	1	1	1
SyncTrigError	0	0	0	0	0	0	0	0
SyncTrig	0	0	0	0	0	0	0	0
EventCounterCleared	0	0	0	0	0	0	0	0
PreCalibrateTrigger	0	0	0	0	0	0	0	0
StackFull	0	0	0	0	0	0	0	0

T69InjectCalibTriggTBMA test description

The T69 test consists in following steps:

1. For each TBM port address 0,1,2,3 set InjectCalibrateTrigger bit for TBMA (write 0x08 in registers E4). Send one L1A trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.

The test report and all fail codes are similar with the ones in T68. The SR1 status byte should be 0xB0, 0xB0, 0x90, 0x90 after each set of InjectCalibrateTrigger bit. The SR1 status byte should be 0xA3 after all four triggers.

For this particular test, we look for the following Header and Trailer bit pattern:

	TBM A				TBM B			
	Port 0	Port 1	Port 2	Port 3	Port 0	Port 1	Port 2	Port 3
EventCounter	13	14	15	16	13	14	15	16
NoTokenPass	0	0	0	0	0	0	0	0
TBMReset	0	0	0	0	0	0	0	0
ROCReset	0	0	0	0	0	0	0	0
SyncTrigError	0	0	0	0	0	0	0	0
SyncTrig	0	0	0	0	0	0	0	0
EventCounterCleared	0	0	0	0	0	0	0	0
PreCalibrateTrigger	1	1	1	1	0	0	0	0
StackFull	0	0	0	0	0	0	0	0

T70InjectCalibTriggTBMB test description

The T70 test consists in following steps:

1. For each TBM port address 0,1,2,3 set InjectCalibrateTrigger bit for TBMB (write 0x08 in registers F4). Send one L1A trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.

The test report and all fail codes are similar with the ones in T69. The SR1 status byte should be 0x90, 0x90, 0xB0, 0xB0 after each set of InjectCalibrateTrigger bit. The SR1 status byte should be 0xA3 after all four triggers.

For this particular test, we look for the following Header and Trailer bit pattern:

	TBM A				TBM B			
	Port 0	Port 1	Port 2	Port 3	Port 0	Port 1	Port 2	Port 3
EventCounter	17	18	19	29	17	18	19	20
NoTokenPass	0	0	0	0	0	0	0	0
TBMReset	0	0	0	0	0	0	0	0
ROCReset	0	0	0	0	0	0	0	0
SyncTrigError	0	0	0	0	0	0	0	0
SyncTrig	0	0	0	0	0	0	0	0
EventCounterCleared	0	0	0	0	0	0	0	0
PreCalibrateTrigger	0	0	0	0	1	1	1	1
StackFull	0	0	0	0	0	0	0	0

T71InjectTBMResetTriggTBMA test description

The T71 test consists in following steps:

1. For each TBM port address 0,1,2,3 set InjectTBMResetTrigger bit for TBMA (write 0x10 in registers E4). Send one L1A trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.

The test report and all fail codes are similar with the ones in T70. The SR1 status byte should be 0x90, 0x90, 0x90, 0x90 after each set of InjectTBMResetTrigger bit. The SR1 status byte should be 0xA3 after all four triggers.

For this particular test, we look for the following Header and Trailer bit pattern:

	TBM A				TBM B			
	Port 0	Port 1	Port 2	Port 3	Port 0	Port 1	Port 2	Port 3
EventCounter	1	1	1	1	21	22	23	24
NoTokenPass	0	0	0	0	0	0	0	0
TBMReset	1	1	1	1	0	0	0	0
ROCReset	0	0	0	0	0	0	0	0
SyncTrigError	0	0	0	0	0	0	0	0
SyncTrig	0	0	0	0	0	0	0	0
EventCounterCleared	0	0	0	0	0	0	0	0
PreCalibrateTrigger	0	0	0	0	0	0	0	0
StackFull	0	0	0	0	0	0	0	0

T72InjectTBMResetTriggTBMB test description

The T72 test consists in following steps:

1. For each TBM port address 0,1,2,3 set InjectTBMResetTrigger bit for TBMB (write 0x10 in registers F4). Send one L1A trigger and monitor response. The monitoring includes the interface board status register SR1 and the TBM analog output digitization.
2. Disconnect TokenOut from TokenIn on both TBMs. Write 0x00 in registers E4, F4.

The test report and all fail codes are similar with the ones in T71. The SR1 status byte should be 0x90, 0x90, 0x90, 0x90 after each set of InjectTBMResetTrigger bit. The SR1 status byte should be 0xA3 after all four triggers.

For this particular test, we look for the following Header and Trailer bit pattern:

	TBM A				TBM B			
	Port 0	Port 1	Port 2	Port 3	Port 0	Port 1	Port 2	Port 3
EventCounter	2	3	4	5	1	1	1	1
NoTokenPass	0	0	0	0	0	0	0	0
TBMReset	0	0	0	0	1	1	1	1
ROCReset	0	0	0	0	0	0	0	0
SyncTrigError	0	0	0	0	0	0	0	0
SyncTrig	0	0	0	0	0	0	0	0
EventCounterCleared	0	0	0	0	0	0	0	0
PreCalibrateTrigger	0	0	0	0	0	0	0	0
StackFull	0	0	0	0	0	0	0	0

T73ClearStackCounter test description

The T73 test consists in following steps:
1. Disable TokenIn for both TBMs. Set PauseReadout bit for both TBMs (write 0x09 in registers E0, F0). Send 5 L1A (Normal) triggers.
2. Read and check StackCounter from both TBMs (write 0xFF in registers E3, F3).
3. Set ClearStack bit for both TBMs (write 0x20 in registers E4, F4).
4. Read and check StackCounter from both TBMs (write 0xFF in registers E3, F3).
5. Enable TokenIn for both TBMs. Reset TBM chip.

The test report looks like the following:

```
**************************************************************
BothTBMs - ClearStackCounter Test Report
ClearStackCounterTest_FailCode=0        0 0 0 0 0 0 0 0 0
**************************************************************
```

The ClearStackCounterTest _FailCode is a 9 bit long integer number:
Bit0= software type error
Bit1= error of return fifo full bit

Bit2= error of return fifo empty bit
Bit3= error of return register address (should be E3 or F3)
Bit4= error of return hub address or port address
Bit5= error of return register data of TBMA read stack counter (should be 0x05)
Bit6= error of return register data of TBMB read stack counter (should be 0x05)
Bit7= error of return register data of TBMA clear stack counter (should be 0x00)
Bit8= error of return register data of TBMB clear stack counter (should be 0x00)

3. Report files description

As briefly stated in Section 1 there are three text files that contain the test program results. The first file, which is associated with each chip, was exemplified extensively in Section 2. There is one more line on this file, at the very end, which summarizes the defects encountered, as follows:

FailCode=27521024 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 0 0 0 1 0 1 1 0 0 0

This is an overall Fail Code, encoded as a 28 bit long integer number. Each bit is set if one or more tests fails. For convenience, a binary representation is also provided, starting with the LSB. The bit encoding is the following:

Bit0= error on T11
Bit1= error on T12
Bit2= error on T13
Bit3= error on T14
Bit4= error on T51
Bit5= error on T52
Bit6= error on T61
Bit7= error on T62
Bit8= reserved
Bit9= reserved
Bit10= reserved
Bit11= reserved
Bit12= error on T67
Bit13= error on T68
Bit14= error on T69
Bit15= error on T70
Bit16= error on T71
Bit17= error on T72
Bit18= error on T73
Bit19= error on T20 or T21 or T22 or T23 or T24
Bit20= error on T25 or T26
Bit21= error on T27 or T28
Bit22= error on T29

Bit23= error on T31 or T32 or T33 or T34
Bit24= error on T35 or T36
Bit25= error on T41 or T42 or T43
Bit26= error on T44 or T45 or T46 or T47
Bit27= error on T48 or T49

The second report file is wafer specific. For example the file named MBFR4GT_WaferData.txt contains brief test results for all chips on wafer ID=MBFR4GT. This is very handy in giving a pass / fail overview of all chips on the specified wafer. Each line summarizes test data for one chip, as in the following example:

9/19/2005	8:06:40 PM	MBFR4GT_1_0	2.486	2.474	2.092	2.053	1.027	1.237	9.85	19.97	0
9/19/2005	8:07:47 PM	MBFR4GT_1_1	2.485	2.479	2.095	2.018	1.027	1.234	9.29	16.83	0
9/19/2005	8:08:56 PM	MBFR4GT_2_0	2.485	2.479	2.094	2.053	1.017	1.228	9.3	16.11	0
9/19/2005	8:10:01 PM	MBFR4GT_2_1	2.485	2.48	2.085	2.027	1.016	1.225	9.2	16.14	0
9/19/2005	8:11:24 PM	MBFR4GT_3_0	2.485	2.475	2.089	2.073	1.027	1.23	9.5	19.95	0

The columns are, from left to right: date, time, wafer ID + reticule# + chip#, the power supply test measurements (see T11 for details) and the above 28 bit long integer that summarizes the overall Fail Code.

The third report file is also wafer specific. For example the file named MBFR4GT_WaferDataAna.txt contains miscellaneous analog tests results for all chips on wafer ID=MBFR4GT. These file is mainly intended for later data analysis. This file was introduced later, after we tested the current 5 wafers. Each line summarizes test data for one chip, as in the following example which shows actually only two lines of this file:

10-3-05	5:14:54 PM	Debug_38_0	2043	2052	2046	1075	1087	1082	
2026	2038	2032	2030	2041	2036	1096	1107	1101	2014
2026	2020	2164	1076	2030	2853	2163	1080	2036	2853
2165	1078	2028	2843	2038	1097	2023	2046	2041	1100
2023	2044	2039	1099	2021	2056	2161	1077	2032	2847
2164	1075	2032	2851	2162	1082	2033	2844	2038	1098
2023	2036	2036	1099	2019	2045	2036	1102	2021	2038
2162	1073	2033	2841	2163	1076	2033	2846	2165	1080
2033	2856	2039	1099	2023	2039	2035	1098	2019	2038
2036	1099	2017	2044	6.05	6.17	6.6	6.82	9.72	10.42	6.1
6.25	6.62	6.9	10.17	10.2	5.95	6.2	6.32	7.02	10.45	11.45
5.82	6.25	6.37	6.45	11.02	10.92	0	25	236	477	764
1054	1376	1712	2046	2377	2696	3002	3286	3560	3797	
3996	4095	0	38	261	504	784	1075	1389	1720	2045
2379	2692	2998	3278	3541	3785	3991	4095			

10-3-05	5:16:55 PM	Debug_39_0	2000	2005	2002	1248	1289	1265	
1990	1997	1994	2015	2018	2017	1265	1305	1282	2001
2007	2004	2027	1440	1985	2155	2097	1066	1992	2492
2180	844	1997	2872	2018	1462	2008	2015	2015	1083
2002	2019	2019	858	2000	2027	2069	1499	2006	2275
2100	1068	1992	2496	2116	773	1978	2640	2020	1516
2011	2020	2018	1082	2005	2019	2015	789	2000	2022
2067	1498	2008	2275	2100	1101	1987	2497	2118	798
1976	2643	2019	1517	2012	2020	2018	1119	2002	2021

2017 817 1996 2020 6.67 6.7 8 8.37 9.65 15.37 6.55
7.32 9.12 8.05 10.77 14.12 7 7.5 8.8 7.97 12.07 15.95
6.67 7.55 7.55 7.22 11.62 17.27 600 663 767 913 1060
1201 1437 1702 1992 2266 2510 2748 2936 3066 3187
3267 3288 730 796 911 997 1141 1313 1520 1777
2025 2274 2503 2693 2878 3015 3072 3199 3291

The columns are, from left to right: date, time, wafer ID + reticule# + chip#, and then a total or 18+72+24+34=148 numbers organized as follows:

1. The first 18 numbers represent, for TBMA (first 9 numbers) and for TBMB (next 9 numbers), the minimum, maximum and average values (over 32 triggers issued in test T34) of the Base Line level, Ultra Black level and AnalogLevel_0 respectively.
2. The next 72 numbers represent data associated with register EA scan (first 24 numbers, see test T41), register EC scan (next 24 numbers, see test T42) and register EE scan (next 24 numbers, see test T43) respectively. Each of the 24 numbers is ordered in 3 groups of 8 numbers, one for each register setting used (0x40, 0x80 and 0xC0 respectively). Each group of 8 numbers contains TBMA values (first 4 numbers) and TBMB values (next 4 numbers) of Base Line, Ultra Black, AnalogLevel_0 and Pulse amplitude respectively.
3. The next 24 numbers are associated with tests T44, T45, T46 and T47 respectively. These numbers are in nanosecond time units. Each group or 6 numbers represents the rising edge and the falling edge time of TBMA Ultra Black , then TBMB Ultra Black and then Pulse Amplitude signals.
4. The last 34 numbers are associated with Pulse Linearity tests for TBMA (first 17, see test T48) and TBMB (next 17, see test T49) respectively. The 17 numbers represent the TBM Pulse amplitude (in ADC counts) for each Pulse setting staring from negative 0x2000 to positive 0x2000 in steps as 0x0400.

4. Wafer testing results

Test results for the 5 mentioned wafers are presented briefly here. There is also an Excel file attached to this document in which all 5 wafers' test data is loaded and some data sorting can be exercised for custom analysis.

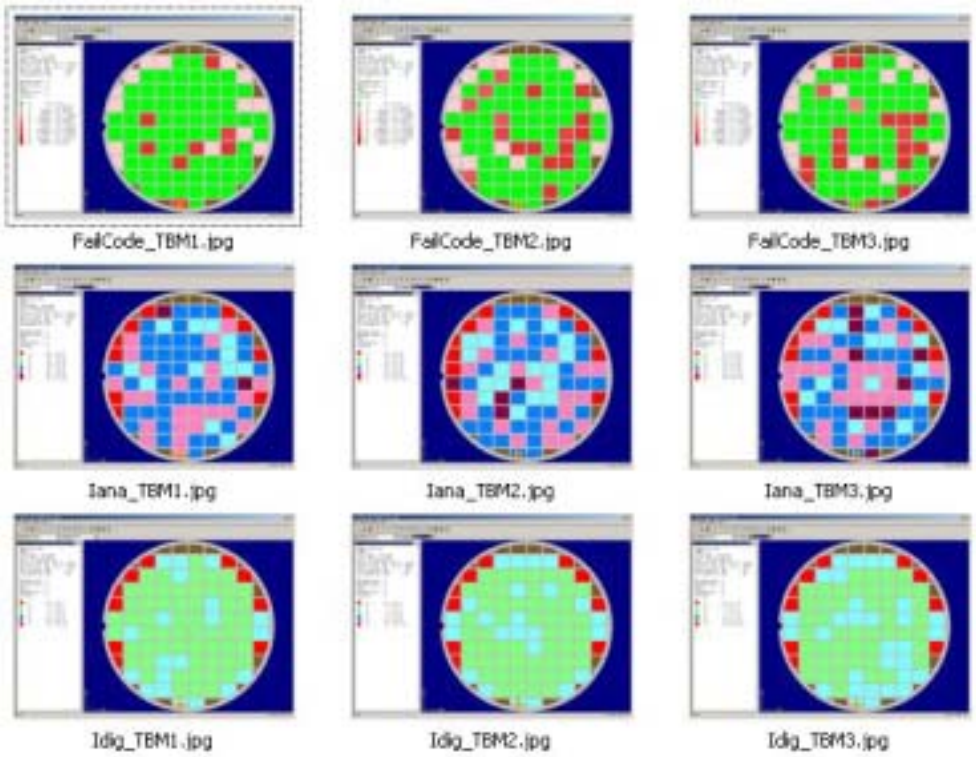
For wafer#1 all six TBM chips inside a reticule were measured. For the other four wafers only two chips per reticule were measured since after wafer dicing the other four chips are lost in order to recover some other (auxiliary) chips included inside the reticule.

Each wafer contains 88 reticules that are probed. The numbering scheme (1 to 88) starts counting the reticules inside a row from left to right, in all rows, starting with bottom row and ending with top row.

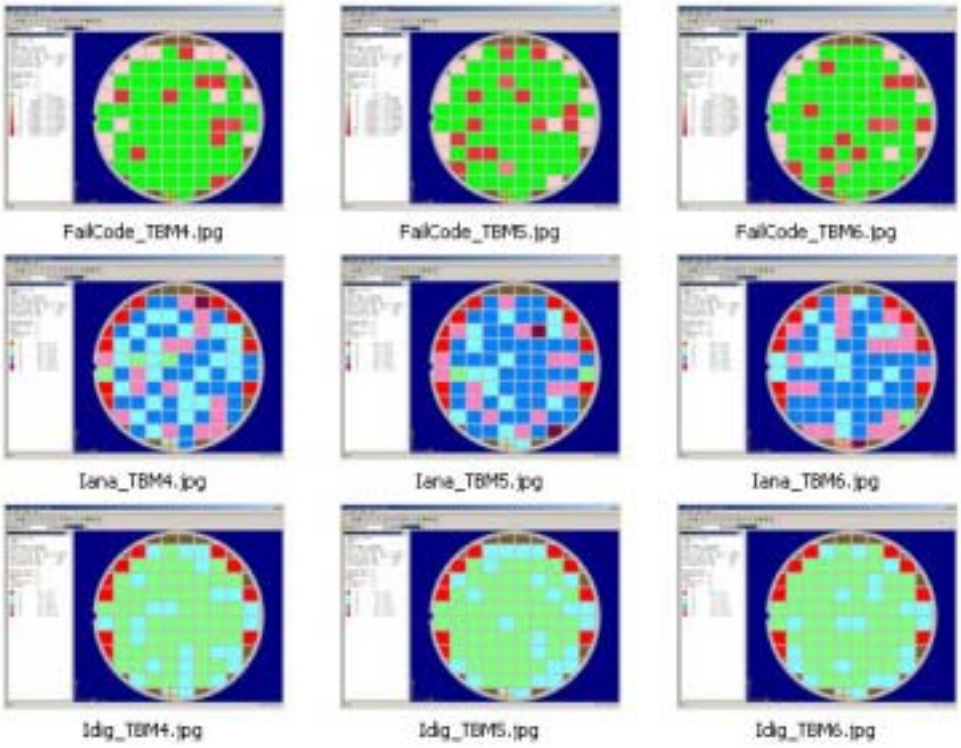
The following pictures are wafer maps generated during the test and showing on wafer distributions of digital and analog current supply and of the 28 bit long integer Fail Code number described in Section 3.

The last next pictures are an example of data analysis performed on the attached Excel file. The TBM gain was defined as the difference between the Base Line and Ultra Black levels. The data was sorted using three criteria: take the chips that pass all tests and sort in ascending order first on TBMA gain, then on TBMB gain.

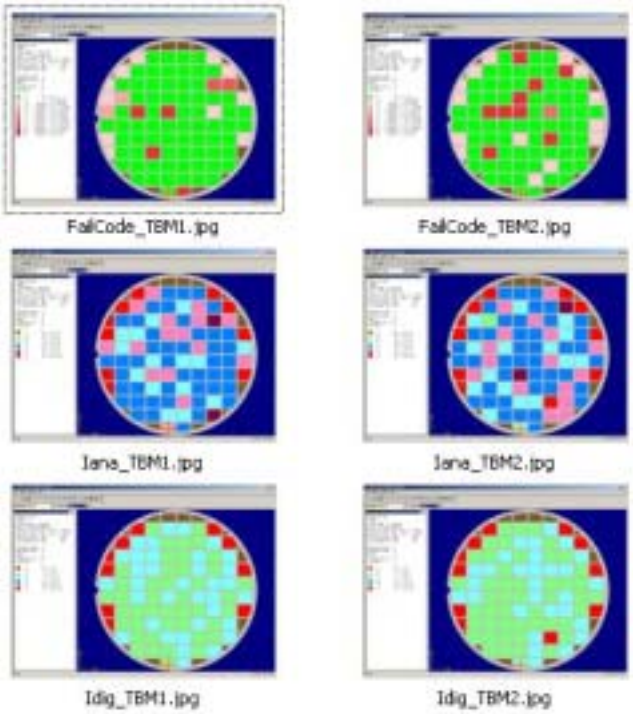
The last five pictures are wafer maps with pass / fail chips (based on the 28 bit long integer Fail Code number) for all five wafers.



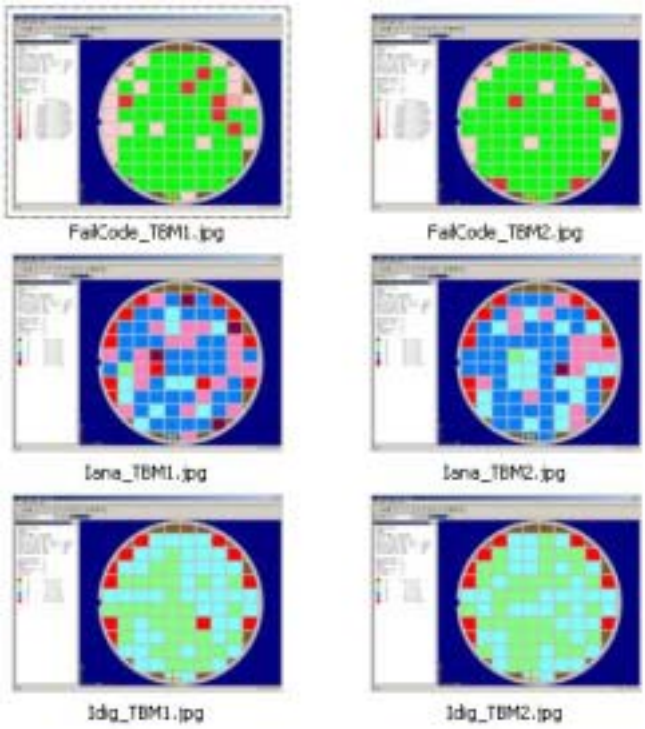
Wafer#1 TBM chips 1, 2 and 3 from reticule



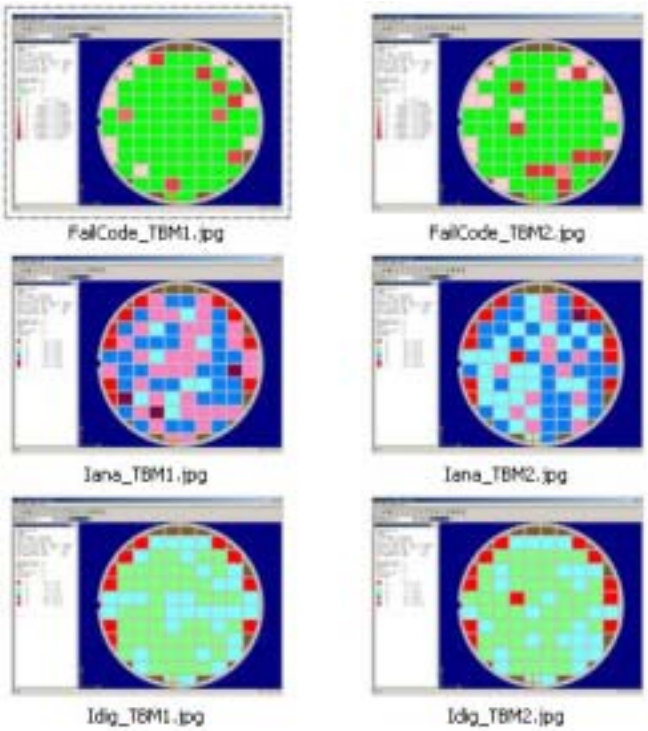
Wafer#1 TBM chips 4, 5 and 6 from reticule



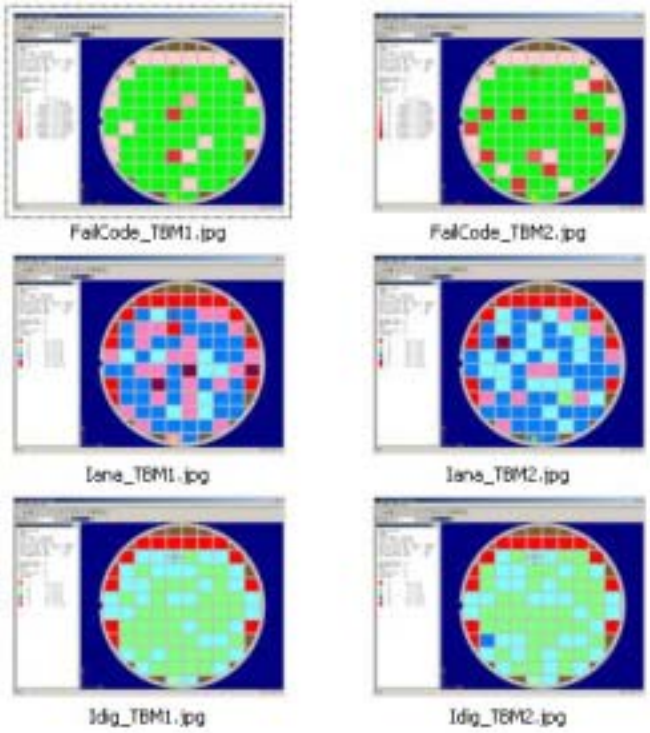
Wafer#2 TBM chips 1 and 2 from reticule



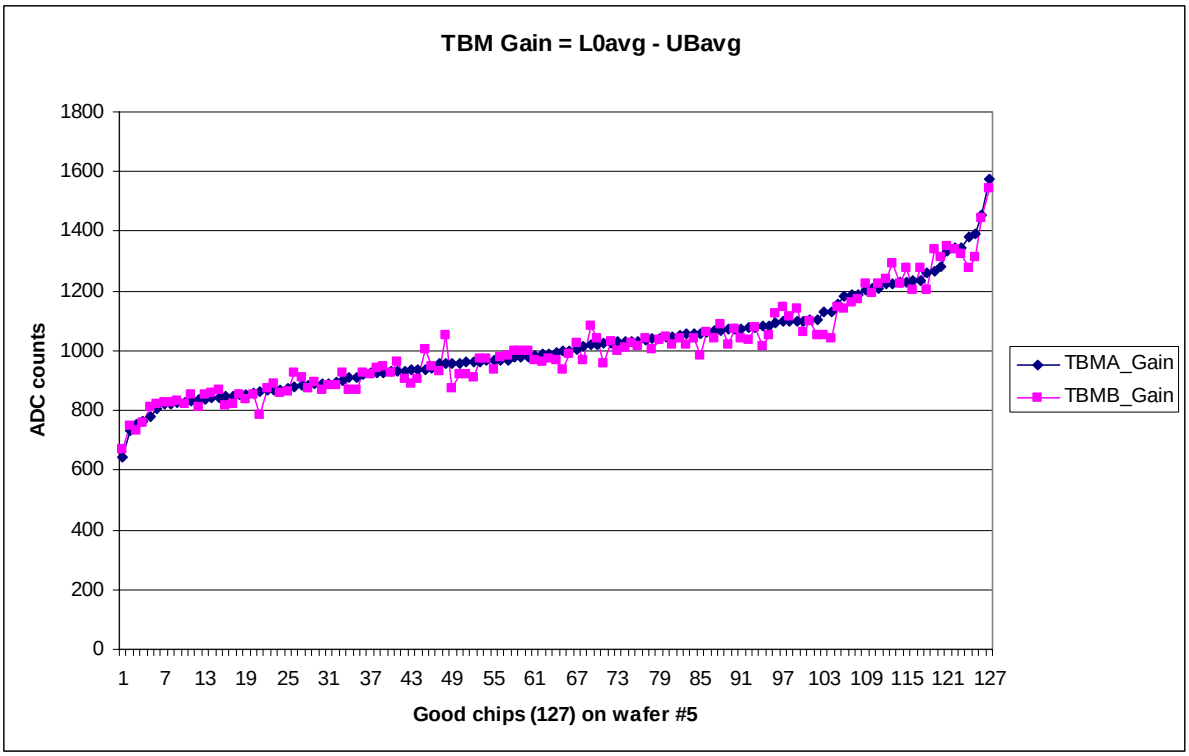
Wafer#3 TBM chips 1 and 2 from reticule

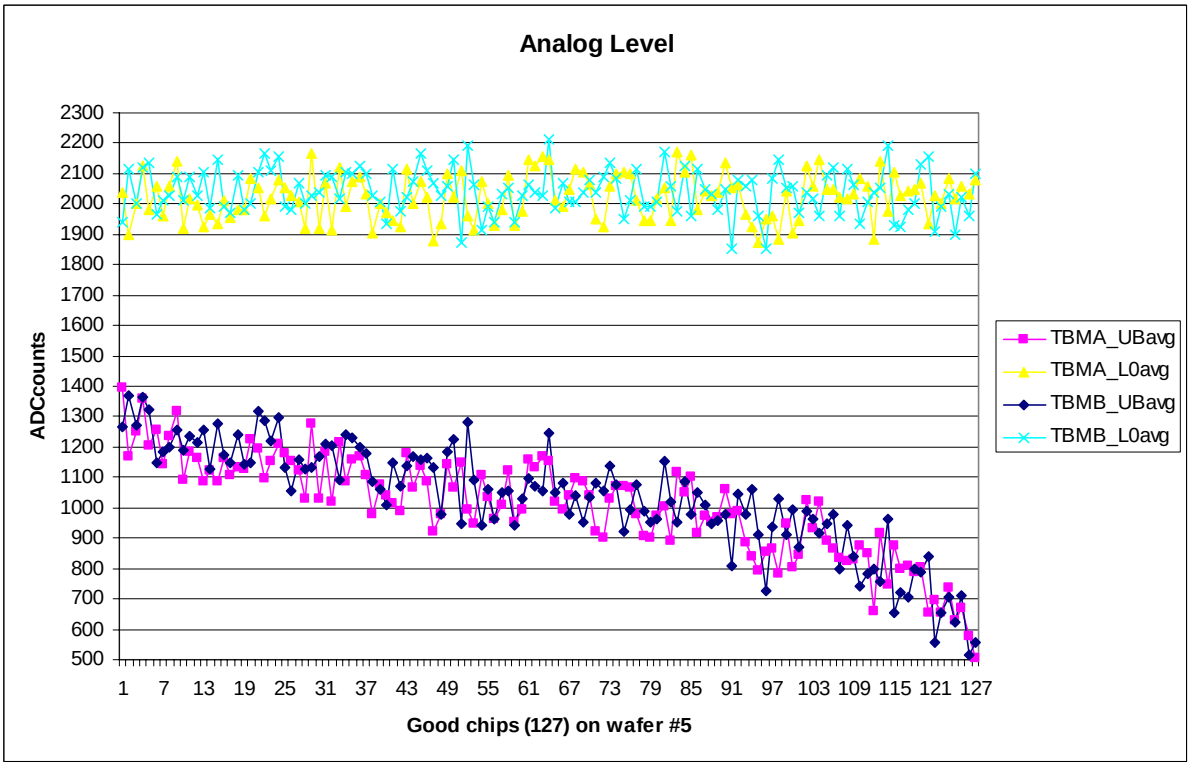


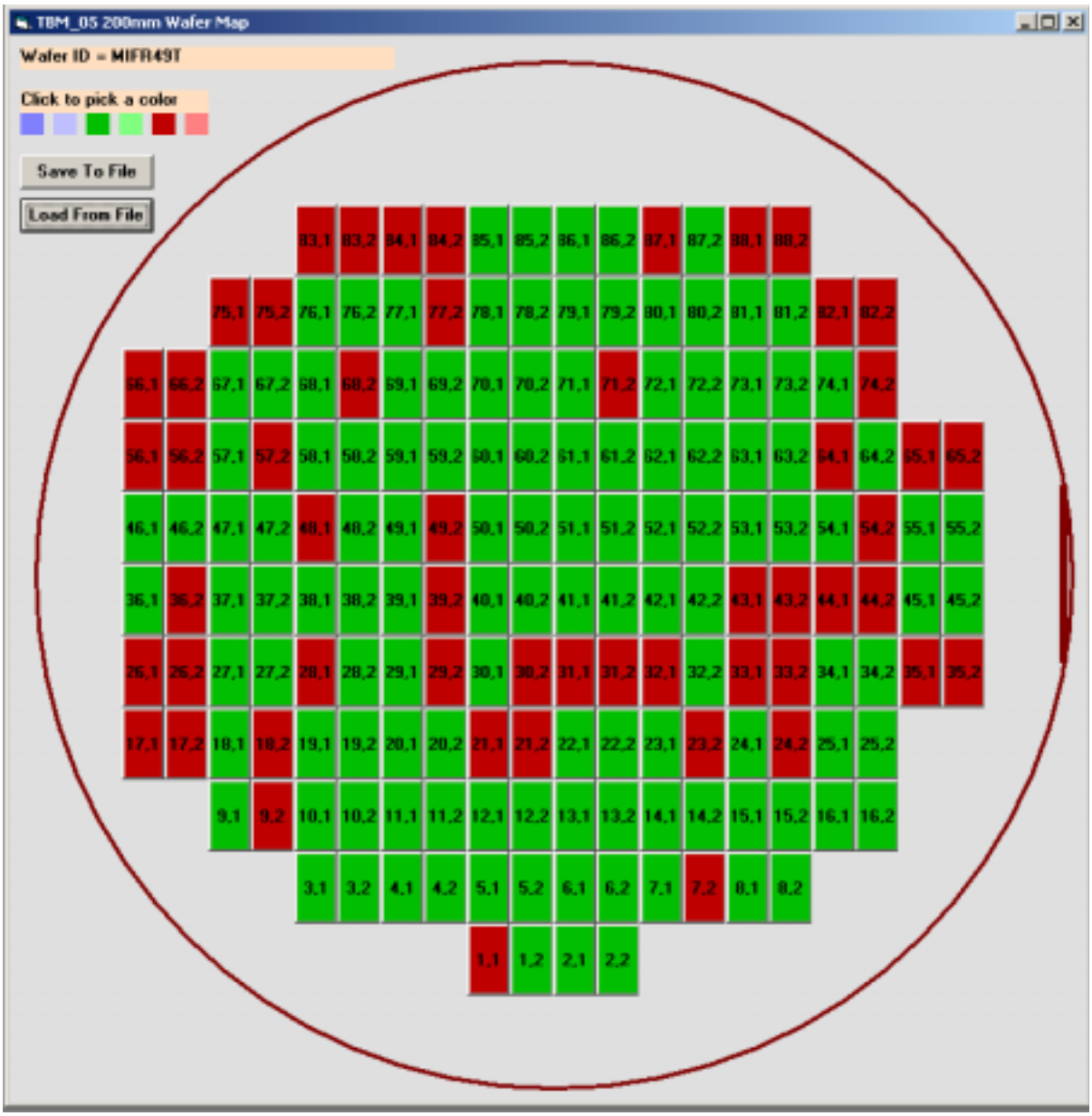
Wafer#4 TBM chips 1 and 2 from reticule



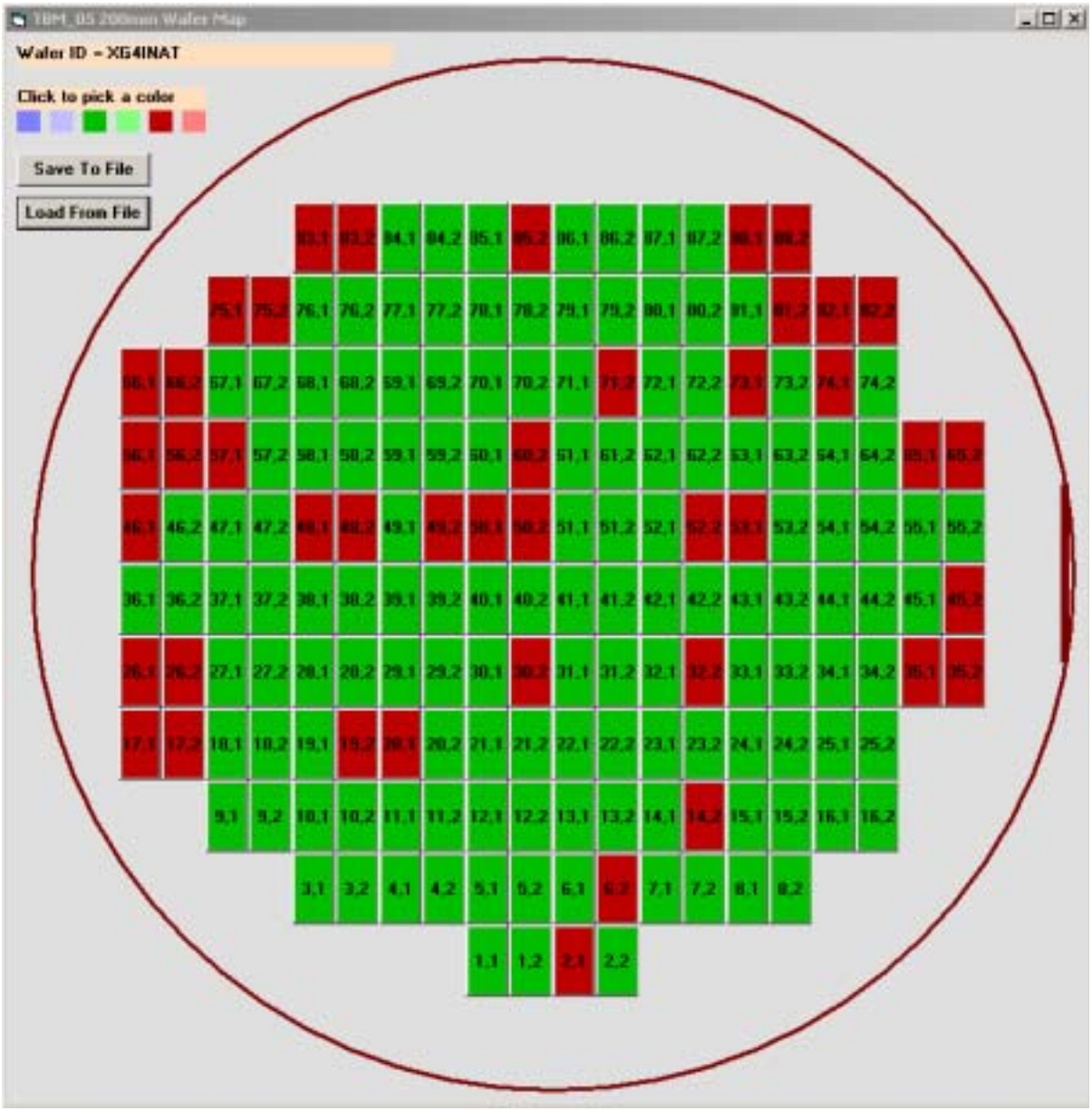
Wafer#5 TBM chips 1 and 2 from reticule


TBM Gain = L0avg - UBavg
ADC counts
0
200
400
600
800
1000
1200
1400
1600
1800
1 7 13 19 25 31 37 43 49 55 61 67 73 79 85 91 97 103 109 115 121 127
Good chips (127) on wafer #5
TBMA_Gain
TBMB_Gain

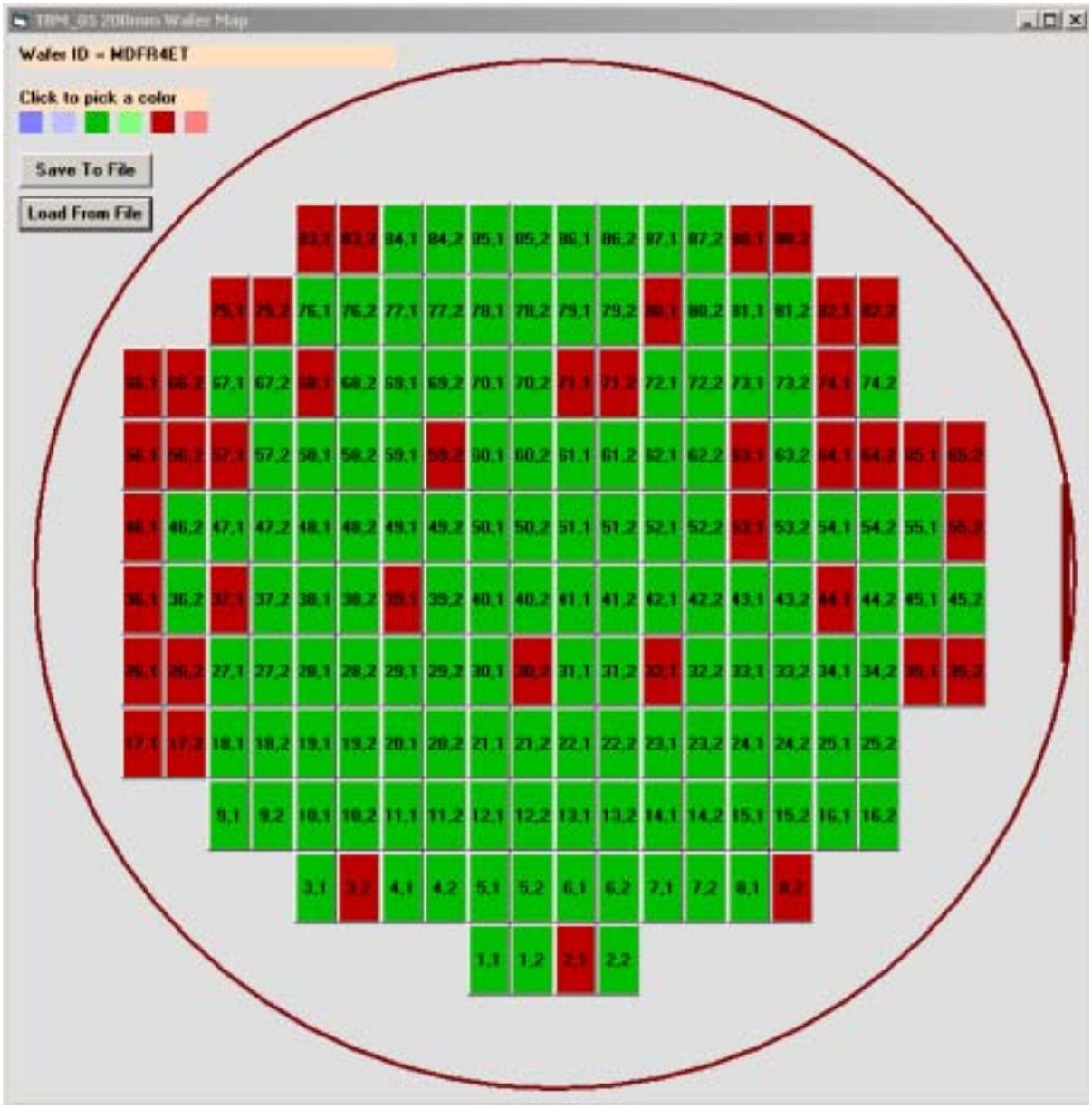

Analog Level
ADCcounts
500
600
700
800
900
1000
1100
1200
1300
1400
1500
1600
1700
1800
1900
2000
2100
2200
2300
1 7 13 19 25 31 37 43 49 55 61 67 73 79 85 91 97 103 109 115 121 127
Good chips (127) on wafer #5
TBMA_UBavg
TBMA_L0avg
TBMB_UBavg
TBMB_L0avg



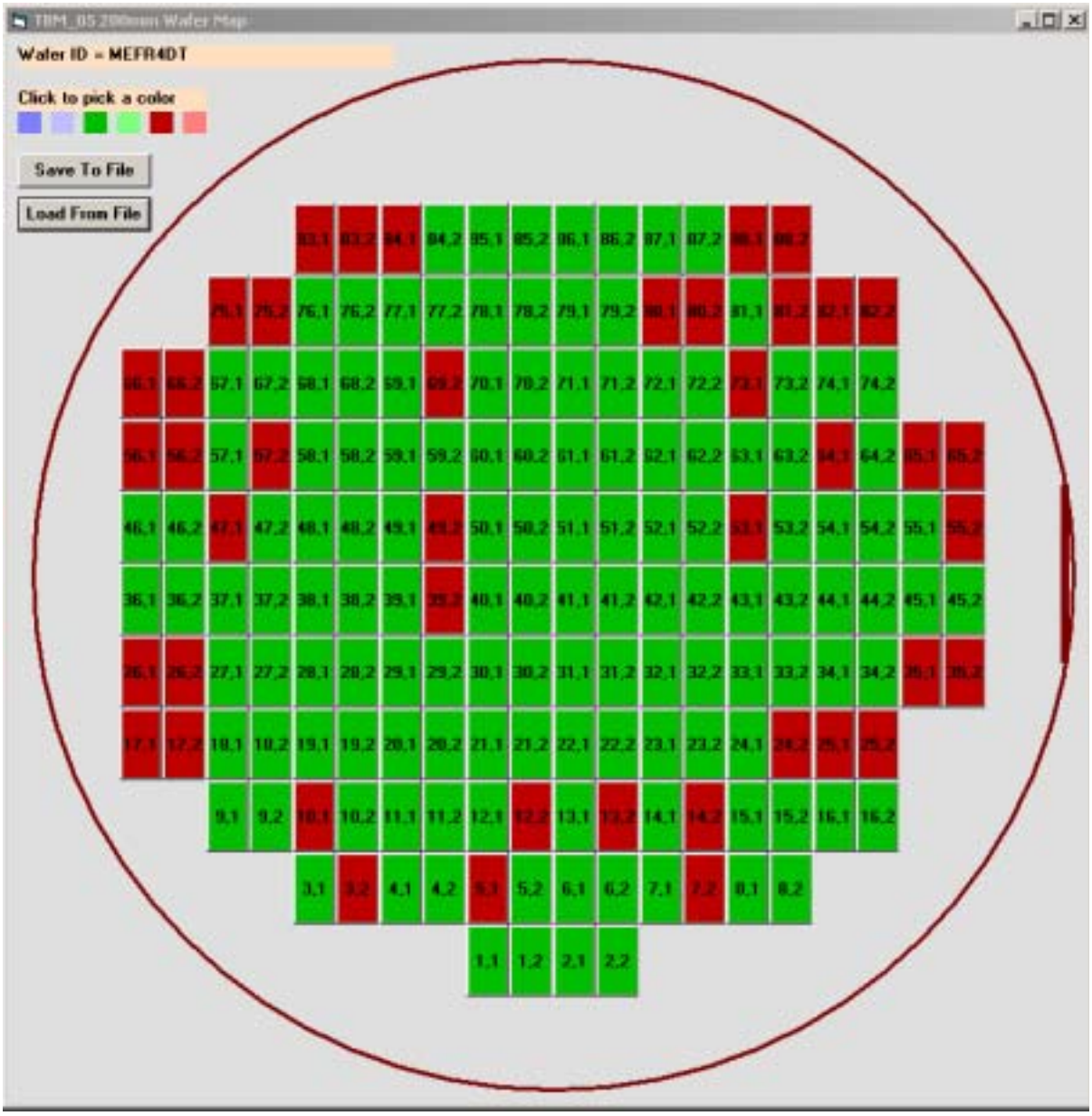
Wafer#1 TBM chips Pass (FailCode=0, green) and Fail (FailCode<>0, red).



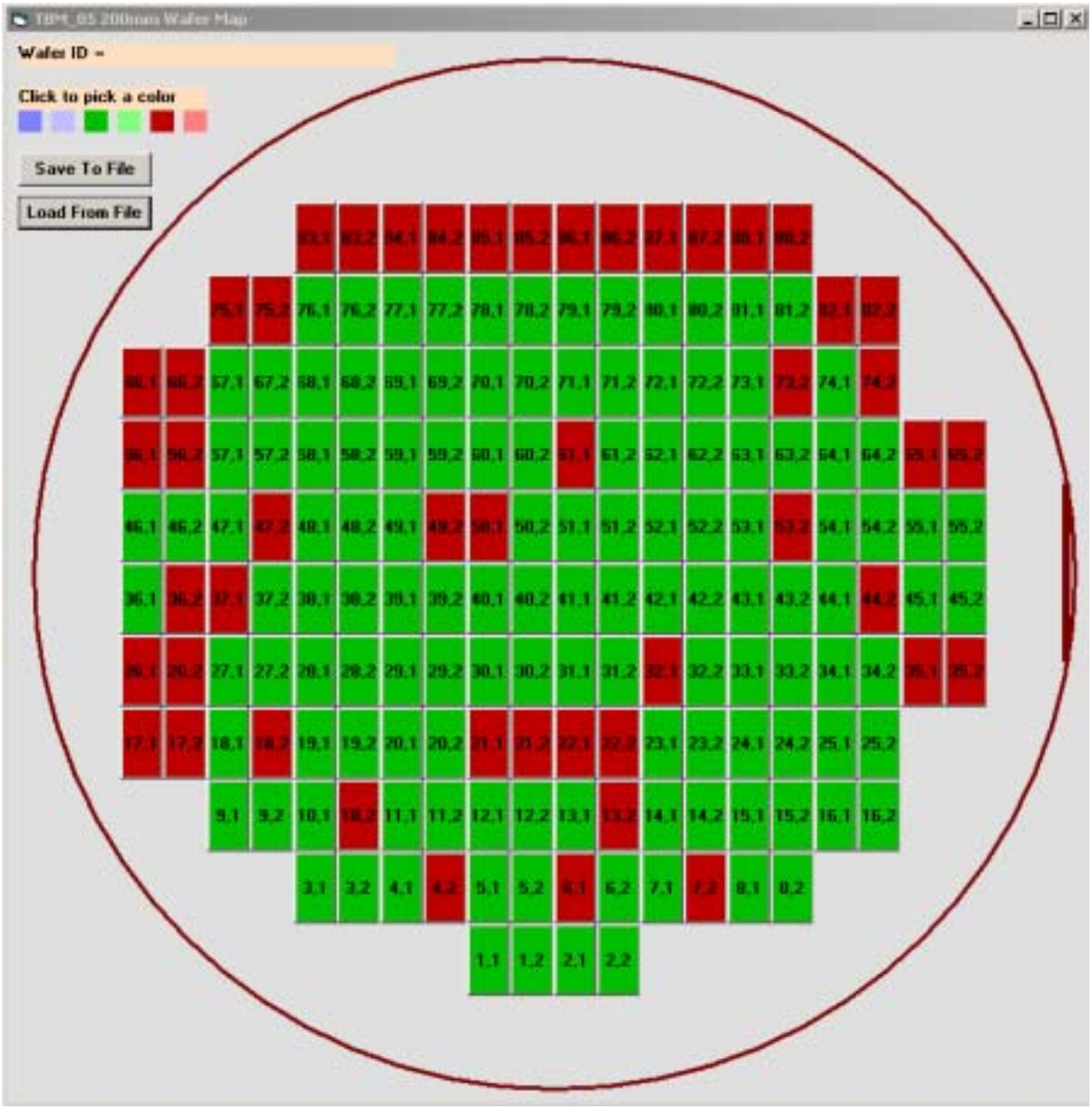
Wafer#2 TBM chips Pass (FailCode=0, green) and Fail (FailCode<>0, red).



Wafer#3 TBM chips Pass (FailCode=0, green) and Fail (FailCode<>0, red).



Wafer#4 TBM chips Pass (FailCode=0, green) and Fail (FailCode<>0, red).



Wafer#5 TBM chips Pass (FailCode=0, green) and Fail (FailCode<>0, red).